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Thermal stability of electrical and structural properties of GaAs-based metal-oxide-semiconductor capacitors with an amorphous $LaAlO_3$ gate oxide

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We report on thermal stability of the electrical and structural properties of metal-oxide-semiconductor capacitors with amorphous $LaAlO_3$ high dielectric constant (high k) oxide on GaAs epitaxial layers with and without an interface amorphous silicon (a-Si) passivation layer to prevent Fermi level pinning at the III-V/high-k interface. The electrical properties of a-Si passivated GaAs improved with annealing temperature, demonstrating reduced equivalent oxide thickness, small ($\sim$50 mV) hysteresis of capacitance-voltage characteristics, and low interface state density ($\leqslant 2\times10^{11}$ eV^{-1} cm^{-2}). Transmission electron microscopy with x-ray microanalysis revealed densification of the amorphous $LaAlO_3$ and its reaction with an oxidized a-Si layer. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2952830]

Motivated by the possibility of obtaining significantly higher effective channel mobility compared to Si-based transistors[1] and reduced gate leakage current,[2] a great deal of attention has recently been devoted to research on group III-V metal-oxide-semiconductor (MOS) devices incorporating high dielectric constant (high k) materials. The key challenge in implementing such MOS devices is the development of a gate dielectric stack that provides a nonpinned Fermi level at the III-V/gate dielectric interface[3,4] and allows a low ($<$1 nm) equivalent oxide thickness (EOT). In addition, to be compatible with the complementary MOS fabrication process, the gate stack and its interface with the III-V semiconductor should be thermally stable in the temperature range needed for the activation of dopants implanted into the source/drain regions. To prevent Fermi level pinning, three major options have been developed for GaAs surface passivation: (1) removal of the native oxide and surface passivation with sulfur prior to *ex situ* high-k deposition,[5] (2) control of oxygen at the III-V interface during *in situ* deposition of Gd_2O_3 or a Ga_2O_3–Gd_2O_3 mixture,[6] and (3) *in situ* deposition of an interface passivation layer (IPL) such as amorphous silicon,[7] germanium,[8] or arsenic.[9] Besides the need to reduce the interface state density to prevent Fermi level pinning, it is also important to avoid the formation of a lower-k oxide between the high-k gate dielectric and the III-V semiconductor to achieve low EOT. From this perspective, a fully *in situ* process of GaAs growth and high-k deposition, or *in situ* deposition of an amorphous arsenic capping layer, which is removed prior to *ex situ* high-k oxide deposition, would appear to be the most attractive options due to the minimal potential contribution of an unintentional interfacial layer to EOT. Nevertheless, as we recently showed, Fermi level pinning can occur during high-k deposition or postdeposition annealing even in a fully *in situ* process of HfO_2 deposition onto GaAs or $In_{0.2}GaAs$. This can be avoided by inserting an ultrathin (0.25–5 nm) amorphous Si (a-Si) passivation layer between the III-V semiconductor and gate oxide.[10] Although, an arsenic capping layer was demonstrated to work efficiently for the *ex situ* deposition of amorphous $LaAlO_3$ on a reconstructed $In_{0.53}GaAs$ surface,[11] the thermal stability of the interfacial properties between the high-k dielectric and III-V semiconductor has not yet been investigated.

In this work, we compare the thermal stability of the electrical and structural properties of the interface between amorphous $LaAlO_3$ and p-type GaAs with and without an a-Si IPL. Our choice of $LaAlO_3$ is motivated by its promising characteristics including a high-k value of $\sim$16,[12] good thermal stability,[13] and reasonable band offsets ($>$1 eV) with Si.[12] The MOS capacitors on GaAs capped with arsenic demonstrated lower EOT compared to a-Si passivated GaAs devices, but revealed strong degradation of the gate leakage after annealing at 700 °C, whereas the devices with amorphous Si remained stable up to 850 °C, exhibited low gate leakage current ($J_G<1$ mA/cm^2 at $V_G=V_{fb}+1$ V), low interface state density ($<2\times10^{11}$ eV^{-1} cm^{-2}), and small ($\sim$50 mV) hysteresis of their C-V characteristics. The capping of a-Si passivated GaAs with arsenic for *ex situ* $LaAlO_3$ deposition allowed us to scale the Si thickness and thus reduce its contribution to EOT. In addition, an appropriate scaling of the a-Si thickness enabled the Si to be kept at the GaAs/$LaAlO_3$ interface,[4] thus preventing its in-diffusion at elevated temperatures.[10]

The samples consisting of a 150 nm thick carbon-doped (2×10^{18} cm^{-3}) buffer layer followed by an 80 nm thick GaAs layer doped with 5×10^{17} carbon/cm^{-3} were grown at U-Albany using a conventional effusion-source molecular beam epitaxy (MBE) reactor (Veeco Modular Gen II) equipped with an As cracker producing As_2 flux. Epitaxial GaAs was grown on heavily doped p-type (001) GaAs substrates at 575 °C and then cooled to 400 °C under the As_2

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flux and further down in vacuum. The surface was maintained arsenic-stabilized as determined by the *in situ* reflection high-energy electron diffraction (RHEED) from the surface reconstruction pattern. For *in situ* passivation, two options were used: (A) *in situ* deposition of amorphous Si followed by capping with arsenic, and (B) arsenic capping only. An amorphous Si layer was grown at ~100 °C. Its thickness ranged from 0.5 to 1.5 nm. The thickness of the arsenic cap deposited on a bare GaAs surface at ~ 20 °C was 22 nm, while on the *a*-Si passivated surface the As_2 layer was expected to be thinner and its density lower than on the bare GaAs surface. The samples were unloaded and transferred to another MBE system (at Penn State University), where the arsenic cap was thermally desorbed in ultrahigh vacuum at 300 °C, and a 2×4 GaAs surface reconstruction was verified by RHEED prior to the deposition of a 20 nm thick amorphous $LaAlO_3$ layer. The amorphous $LaAlO_3$ layer was deposited at ~100 °C in molecular oxygen at a background pressure of 2×10^{-6} Torr, followed by *in situ* annealing at ~340 °C in a mixture of molecular oxygen and ozone (~10%) at the same background pressure. A 200 nm thick TaN metal gate was then deposited *ex situ* by the physical vapor deposition following either postdeposition annealing (PDA) or followed by postmetallization annealing (PMA) in the temperature range of 600–900 °C for 5 min in a nitrogen ambient. The MOS capacitors (MOSCAPs) were completed by patterning the gate stack using photolithography and reactive ion etching and making the backside Ohmic contact by In soldering. The capacitance-voltage (*C-V*) and current-voltage (*I-V*) characteristics were measured using HP4195 and HP4192A characterization tools. The structural and chemical properties of the GaAs/$LaAlO_3$ interface were studied by transmission electron microscopy (TEM) using a JEOL FEG 2010 microscope with energy dispersive x-ray analysis (EDX).

Figure 1(a) compares high frequency capacitance-voltage characteristics of the GaAs MOSCAPs with 1.5, 0.5, and 0 nm thick *a*-Si IPLs after PMA at 600 °C. All samples demonstrate sharp transitions from depletion to accumulation and low frequency dispersion of the accumulation capacitance (less than 3%/decade in the range from 100 Hz to 1 MHz). The EOT evaluated from the accumulation capacitance for these samples is 7.7, 6.4, and 5.4 nm, respectively. Data from the sample without *a*-Si IPL indicate that the *k*-value of our amorphous $LaAlO_3$ is ~15, in agreement with published data.[13] The difference in the EOT of the samples with and without the passivation layer implies that the *a*-Si IPL is fully oxidized and its contribution to EOT can be expressed as

$$\mathrm{EOT} = k_{\mathrm{SiO_2}}\left(\frac{t_{\mathrm{LaAlO_3}}}{k_{\mathrm{LaAlO_3}}} + \frac{t_{\mathrm{IPL}}}{k_{\mathrm{IPL}}}\right), \quad (1)$$

where $t_{\mathrm{LaAlO_3}}$ and t_{IPL} are thicknesses and $k_{\mathrm{LaAlO_3}}$ and k_{IPL} are dielectric constants of $LaAlO_3$ and oxidized *a*-Si IPL layers, respectively, and k_{IPL} is close to $k_{\mathrm{SiO_2}}=3.9$. The inset in Fig. 1(a) shows *I-V* characteristics obtained on the GaAs MOSCAPs with and without *a*-Si IPL. The gate leakage current of the sample with fully oxidized Si gradually increases with temperature, but remains low ($J_G<1$ mA/cm^2 at $V_G=V_{\mathrm{fb}}+1$) after a PDA at 800 °C, while on the samples without Si an increase of the leakage current by approximately three orders of magnitude occurs even after 700 °C anneal resulting in strong degradation of the *C-V* characteristics. The electrical properties and thermal stability of the GaAs MOSCAPs with *a*-Si IPLs essentially depends on the oxidation state of the *a*-Si layer. Its excess oxidation leads to formation of As–O bonds resulting in formation of the traps and Fermi level pinning at the GaAs/high-*k* interface. This was demonstrated in Ref. 7 when the *a*-Si layer exposed to air was thinner than 1.5 nm. On the other hand, insufficient oxidation of the *a*-Si layer results in Si in-diffusion during high temperature annealing. We recently showed that using *in situ* high-*k* oxide deposition where Si oxidation within processing steps was accurately and reproducibly controlled, in-diffusion of Si was suppressed when the Si IPL thickness was thin enough (<0.5 nm) to be completely oxidized. Similar behavior is observed in the present work for the GaAs samples with *a*-Si and *ex situ* deposited $LaAlO_3$. Using an As_2 protective layer to prevent the *a*-Si layer from excess oxidation during air exposure the Si thickness can be reduced to 0.5 nm. Reducing the air exposure time for a thicker *a*-Si layer results in its incomplete oxidation and in-diffusion at 700 °C as clearly indicated by inversion of the conductivity type, see Fig. 1(b). In contrast, the sample with a fully oxidized *a*-Si layer exhibits unchanged *p*-type conductivity behavior up to 850 °C. In addition to good thermal stability of the sample with fully oxidized *a*-Si, increasing the annealing temperature leads to progressive improvement of both the high-*k* stack and interface quality, as can be seen from Fig. 2: after annealing at 800 °C the accumulation capacitance increases by more than 50% as compared to 600 °C, while hysteresis is reduced from ~1 V to ~50 mV [Fig. 2(a)]; *C-V* stretch-out ($\Delta C/\Delta V$) is improved by a factor of ~2.3, and the midgap interface state density determined by both the Terman and conductance techniques is found to be less than 2×10^{11} cm^{-2} eV^{-1} [Fig. 2(b)]. Increasing the PDA tem-

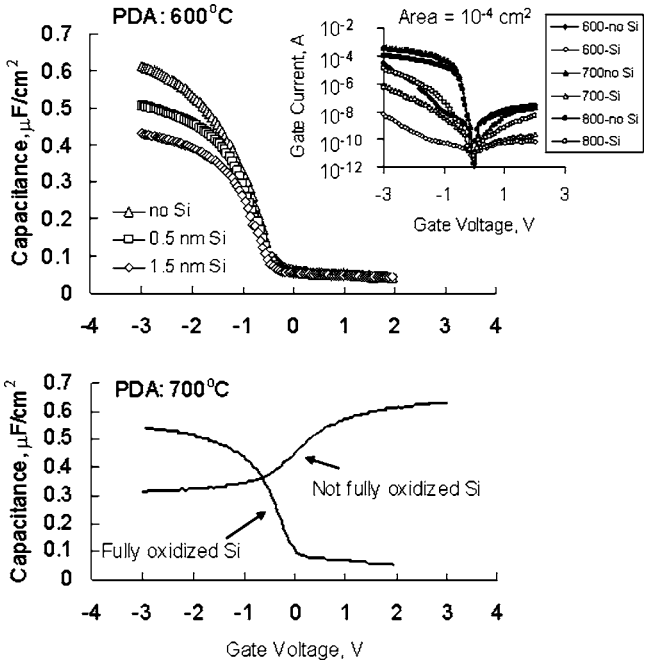

FIG. 1. (a) High frequency (1 MHz) *C-V* characteristics measured on GaAs MOSCAPs with and without *a*-Si IPL after PDA at 600 °C. The inset compares *I-V* characteristics obtained after annealing at various temperatures. (b) *C-V* characteristics on GaAs with fully oxidized and not fully oxidized *a*-Si IPLs after PDA at 700 °C.

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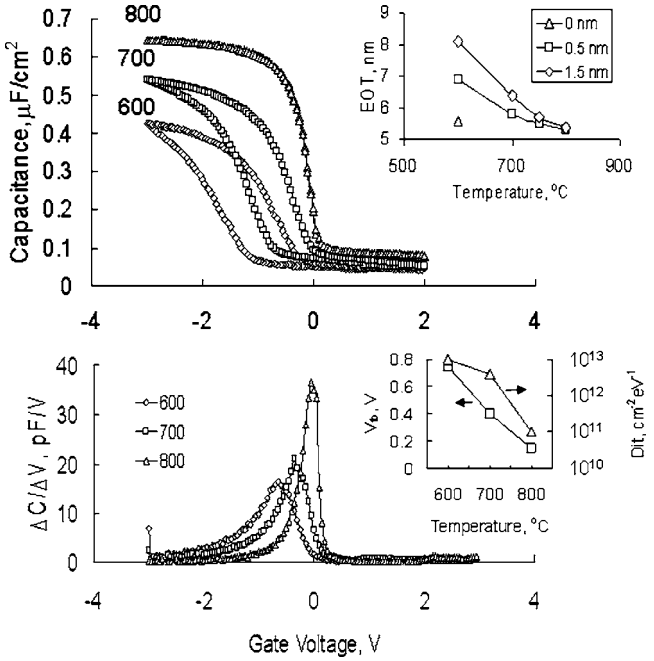

FIG. 2. (a) Effect of annealing on the *C-V* characteristics of GaAs MOSCAP with a 1.5 nm thick fully oxidized *a*-Si IPL. The inset shows the contribution of the *a*-Si to EOT at various temperatures. (b) The improvement of *C-V* stretch out with PDA temperature. The inset shows the annealing dependence of V_{fb} and D_{it}.

perature also results in a notable reduction of the flat band voltage V_{fb}, as shown in inset of Fig. 2(b).

To understand the role of the *a*-Si IPL in both EOT reduction and thermal stability of the gate leakage, we performed TEM/EDX analyses on the GaAs sample with a fully oxidized 1.5 nm thick Si layer. It is seen from the cross-sectional high-resolution TEM images shown in Fig. 3(a), that after annealing at 600 °C the total oxide thickness is ~20 nm, while after 800 °C it is reduced to ~15 nm, see Fig. 3(b). The EDX data obtained by line scanning across the interface indicates that the La/Al peaks and the Si peak are clearly separated after annealing at 600 °C, as shown by arrow in Fig. 3(c), whereas after 800 °C the Si profile overlaps with the La/Al peaks, as seen from Fig. 3(d). The La based oxides are known to have a large driving force to react with SiO_x to form silicates.[14] The observed shift in the Si profile in the Fig. 3 implies that such reaction occurs upon high temperature annealing. Remarkably, diffusion of SiO_x

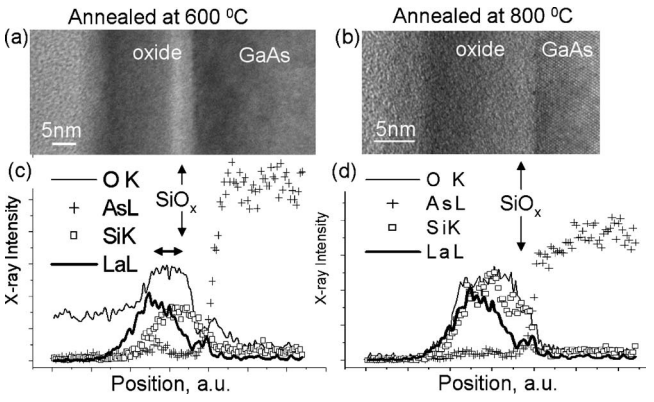

FIG. 3. Cross-sectional TEM/EDX data obtained on GaAs with a fully oxidized 1.5 nm thick *a*-Si layer and a 20 nm thick $LaAlO_3$ layer after annealing at 600 °C (left) and 800 °C (right).

into amorphous $LaAlO_3$ takes place without degradation of GaAs/oxide interface or noticeable (via electrical measurements) diffusion of any species into the semiconductor. The observed dissolving of low-*k* SiO_x layer into $LaAlO_3$ at higher temperatures can readily explain increasing of accumulation capacitance and reduction of EOT with annealing observed in the Fig. 2(a). After high temperature annealing, the contribution of the SiO_x layer into EOT is reduced. At the same time, the $LaAlO_3$ thickness is reduced manifesting densification of the layer. The latter process calls for a slight reduction of the oxide *k*-value down to ~11.5 as estimated from the Eq. (1) that is likely due to intermixing with silicon oxide. The presence of the interfacial SiO_x layer also accounts for the lower gate oxide leakage current[2] and its stability up to 850 °C where this layer disappears.

In summary, we have investigated thermal stability of the electrical and structural properties of MOS capacitors with amorphous $LaAlO_3$ on GaAs with and without *a*-Si passivation layer. Although, MOS capacitors without *a*-Si IPL demonstrated lower EOT than the Si-passivated samples, strong degradation of the gate leakage current after anneal at 700 °C on nonpassivated samples makes this approach not feasible. In contrast, *a*-Si passivated GaAs exhibited not only excellent thermal stability of the electrical and structural properties up to 800 °C, but also significant improvement of both the high-*k* oxide and interface properties with annealing temperature demonstrating a reduction of EOT by ~50%, a reduction of hysteresis by 20 fold, and a low interface state density of $<2\times10^{11}$ eV^{-1} cm^{-2}. Good thermal stability of the $LaAlO_3$/GaAs interface along with strong potential for scalability of the EOT at low gate leakage current makes it suitable for the gate-first surface channel MOSFET applications.

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