Comparative electron spin resonance study of epi-Lu$_2$O$_3$/(111)Si and a-Lu$_2$O$_3$/(100)Si interfaces: Misfit point defects

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An electron spin resonance study has been carried out on heteroepitaxial Si/insulator structures obtained through growth of epi-Lu$_2$O$_3$ films on (111)Si ($\sim$4.5% mismatch) by molecular-beam epitaxy, with special attention to the inherent quality as well as the thermal stability of interfaces, monitored through occurring paramagnetic point defects. This indicates the presence, in the as-grown state, of P$_b$ defects ($\sim 5 \times 10^{11}$ cm^{-2}) with the unpaired sp^3 Si dangling bond along the [111] interface normal, the archetypical defect (trap) of the standard thermal (111)Si/SiO$_2$ interface, directly revealing, and identified as the result of, imperfect epitaxy. The occurrence of P$_b$ defects, a major system of electrically detrimental interface traps, is ascribed to lattice mismatch with related introduction of misfit dislocations. This interface nature appears to persist for annealing in vacuum up to a temperature T$_{an}$$\sim$420 °C. Yet, in the range T$_{an}$$\sim$420–550 °C, the interface starts to "degrade" to standard Si/SiO$_2$ properties, as indicated by the gradually increasing P$_b$ density and attendant appearance of the EX center, an SiO$_2$-associated defect. At T$_{an}$$\sim$700 °C, [P$_b$] has increased to about 1.3 times the value for standard thermal (111)Si/SiO$_2$, to remain constant up to T$_{an}$$\sim$1000 °C, indicative of an unaltered interface structure. Annealing at T$_{an}$$>$1000 °C results in disintegration altogether of the Si/SiO$_2$-type interface. Passivation anneal in H$_2$ (405 °C) alarmingly fails to deactivate the P$_b$ system to the device grade (sub) 10^{10} cm^{-2} eV^{-1} level, which would disfavor c-Lu$_2$O$_3$ as a suitable future high-κ replacement for the a-SiO$_2$ gate dielectric. Comparison of the thermal stability of the c-Lu$_2$O$_3$/(111)Si interface with that of molecular-beam deposited amorphous-Lu$_2$O$_3$/(100)Si shows the former to be superior, yet unlikely to meet technological thermal budget requirements. No Lu$_2$O$_3$-specific point defects could be observed. © *2010 American Institute of Physics.* [doi:10.1063/1.3326516]

I. INTRODUCTION

The continuous downscaling of Si-based complementary metal oxide semiconductor (CMOS) device dimensions has met the incessant demand for increased performance of microelectronic devices for decades. Now, the native oxide of Si, a-SiO$_2$, with thicknesses reducing down to the 1 nm range is nearing its fundamental limits as a gate dielectric leading to major problems such as unacceptably enhanced leakage current and increased failure probabilities.[1,2] This has brought about an impressively intense research for replacement by an insulator of higher dielectric constant κ [$\gg \kappa$(SiO$_2$)=3.9], since these insulators allow for a physical thicker layer while maintaining high capacitance. Various metal oxides, such as HfO$_2$, ZrO$_2$, and Al$_2$O$_3$ have been extensively investigated because of their high-κ and appropriate high energy barriers at the interface for electrons and holes in Si.[3,4] Currently, the HfO$_2$-based insulators, including HfSi$_x$O$_y$N$_z$, are emerging as leading contenders, and in fact have recently been introduced in devices.[5] Rare earth (RE) oxides, such as Lu$_2$O$_3$, Gd$_2$O$_3$, and La$_2$O$_3$ are also promising candidates for the next generation of metal-oxide-semiconductor field effect transistors because of their large band gap, high-κ, and low leakage current.[6–8]

Besides exhibiting a high operational dielectric constant, a dielectric material must satisfy many more criteria to be suitable to replace SiO$_2$ as gate dielectric. One unconditional requirement is realization of a high quality Si/high-κ interface, equivalent to, or possibly even surpassing, the superb Si/SiO$_2$ one, since it fundamentally affects device performance. Typically, deposition of a high-κ metal oxide directly on Si results in the formation of a SiO$_x$ interlayer (IL), reducing the global capacitance of the CMOS conductivity channel, that is, increase of the capacitance equivalent thickness (CET) t$_{eq}$. This interfacial layer has been revealed by numerous microstructural imaging/analysis techniques such as medium-energy ion scattering, high-resolution transmission electron spectroscopy (HRTEM), and x-ray photoelectron spectroscopy (XPS).[1,3,9] The SiO$_x$ IL formation was demonstrated long ago on the atomic scale by electron spin resonance (ESR) studies,[10] which revealed the presence at the Si/insulator interface of Si dangling bond (DB)-type point defects, termed P$_b$-type centers. It has since been affirmed by independent ESR studies.[11–15] Since in modern device fabrication, the dielectric material is deposited in the middle of the processing sequence with several high-

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temperature (T) anneals applied afterwards, the thermal stability of these newly conceived Si/high-κ interfaces comes as one more issue.

So, given the endemic character of $SiO_{2(x)}$ IL formation for Si/high-κ metal oxide systems, its occurrence may be turned to a potential bonus in that it may enable to realize an interface of superb electronic quality. And in fact, the introduction of a tightly thickness controlled $SiO_{2(x)}$ IL of minimal thickness is currently adapted as a *modus vivendi* route in progress,[16,17] also in connection with the HfO_2-based insulators taken into production. But obviously, its presence conflicts with CET optimization restrictions, so its formation should ideally be avoided during insulator/Si heterostructure growth and creation suppressed (prevented) during necessary post growth thermal treatments. Obviously, a main burden of quality will then rest with the newly formed interface, that is, establishing a high quality interface in terms of (absence of) detrimental interface traps. In addition to no IL formation, this comes as a major requirement for a dielectric suitable to replace SiO_2.

In view of these requirements, Lu_2O_3 would appear a suitable candidate for the replacement of SiO_2. Despite its rather moderate $\kappa \sim 12$,[18–20] Lu_2O_3 offers several advantages, like a wide band gap ($\sim 5.8 \pm 0.1$ eV) (Ref. 21) and a symmetric band alignment at the interface with Si, i.e., conduction and valence band offset of 2.1 ± 0.1 and 2.6 ± 0.1 eV,[21] respectively. The density of interface traps should be limited at the Lu_2O_3/Si interface, due to the intrinsic high energy of the $5d$ shell of Lu and its low occupancy.[22]

Concerning the thermodynamic stability of Lu_2O_3 in contact with Si, different studies have been published. Hubbard and Schlom[23] showed, using Gibbs free energy calculations, that Lu_2O_3 in contact with Si should be stable against silica formation. For stability against silicide and silicate formation no calculations were done due to the lack of relevant thermodynamic data. Using a newly developed depth profiling extended angle-resolved photoelectron spectroscopy, Nohira *et al.*[16] investigated the chemical composition of the IL layer formed between (100)Si and amorphous (a)-Lu_2O_3 films grown by electron beam evaporation, concluding the IL to be Lu-silicatelike. Marsella and Fiorentini[24] studied the thermal stability of La_2O_3, ytterbia, Lu_2O_3, and Y_2O_3, in contact with Si through *ab initio* enthalpy calculations. They found these oxides to be stable against silica and silicide formation, yet not silicates, in line with the experimental results obtained by Nohira *et al.*[16] In subsequent experimental work,[18] a-Lu_2O_3 was grown on (100)Si by atomic layer deposition (ALD). An SiO_2 IL (thickness $d_{SiO_2} \sim 1.1$ nm) was observed in the film in its as-deposited state, which grew to 3.5 nm after an anneal at 950 °C in N_2 for 60 s. These changes in interfacial properties after annealing strongly affected the CET of the entire gate stack. Darmawan *et al.*,[6] by contrast, were able to grow an a-Lu_2O_3 film on (100)Si using the pulsed-laser deposition technique, apparently without the formation of a SiO_2 IL, as evidenced by HRTEM images. Even after a postdeposition anneal (PDA) at $T_{an} \sim 600$ °C in N_2 no SiO_2 IL formation was observed by HRTEM. Later, Zenkevich *et al.*[25] investigated the effects of PDA on the

chemical composition and electrical properties of ultrathin (~ 2–5 nm) a-Lu oxide layers grown on chemically oxidized (100)Si. They observed, in agreement with theoretical results[24] that within the $Lu_2O_3/SiO_2/Si$ structure the Lu_2O_3 is not stable against silicate formation under vacuum annealing at $T_{an} \geq 900$ °C.

II. HIGH-κ INSULATOR/SI INTERFACES

A. Crystalline high-κ layers

Generally, scientific work has focused on the use of *amorphous* high-κ materials to replace a-SiO_2, although an inherent property of a solid amorphous/crystalline interface is point defect formation—at the origin of detrimental charge traps and recombination centers, as a result of stress-related lattice-network mismatch, aided by steric hindrance and difference in bond coordination. In contrast, less effort has been devoted to the "opposite" solution, i.e., growing epitaxial oxides bearing the potential of ultimate gate stack scaling through the ability to establish truly atomically abrupt interfaces with c-Si, maximum κ-value, IL-free interfaces, and offer opportunities to eliminate interface states (imperfections) through optimized interface engineering. The epitaxial growth of oxides on Si dates back to the pioneering work of Ihara *et al.*[26] (1982) reporting on the epitaxial growth of MgO and Al_2O_3 on Si. Later, Kada and Arita were probably the first to succeed in growing a crystalline mixed metal oxide as a monolithic, commensurate lattice matched structure on (111)Si, i.e., $Sr_xBr_{1-x}O$ with the best result obtained for x=0.32 grown in the range 780–850 °C; in a next step, epitaxial $Si/Sr_xBr_{1-x}O/(111)Si$ structures were grown.[27] Within the context of the current study focusing on RE oxides on Si, this was followed by pioneering works dealing with the epigrowth of Y_2O_3,[28] CeO_2,[29] Pr_2O_3,[30] Gd_2O_3,[31] and Sc_2O_3.[32] Later, numerous works appeared dealing with various aspects of sample growth and quality (see, e.g., Refs. 33–36). As to the aimed application in semiconductor device technology, the achieved quality of the oxide/semiconductor entity, in particular the epioxide/Si interface, is of crucial importance. In this respect, though concerning a non-RE oxide, noteworthy appears the work of McKee *et al.*[37] reporting on the growth of high quality commensurate $SiTiO_3$ perovskite ($\kappa \approx 80$) on (100)Si with combined electrical performance analysis: a Pt/epi-$SrTiO_3$(15 nm)/(100)Si capacitor yielded the result of $t_{eq} < 10$ Å, which clearly demonstrated that crystalline oxides on Si do offer the opportunity for a fundamental change in device physics for future semiconductor technology. Since then, several studies were devoted to the epitaxial growth of RE oxides of the cubic bixbyite Mn_2O_3 structure on Si in conjunction with electrical/device quality probing to various extend.[38–40] For some RE oxides like CeO_2, Pr_2O_3, and Sc_2O_3 directly grown on Si, no SiO_x IL was observed.[32,33,35,36]

The case of CeO_2, being a RE oxide of nonbixbyite structure, may appear distinct, yet it is addressed here for reasons of comparison. In contrast to the RE oxides, calculations indicate the CeO_2/Si entity not to be thermodynamically stable,[23] as supported by experimental data. A notable result came from Nishikawa *et al.*,[36] who compared metal-

insulator-semiconductor field-effect transistors (MISFETs) made using CeO_2 epitaxially grown directly on (111)Si (no IL observed), with those grown with a Ce silicate IL. To obtain direct growth of CeO_2 on (111)Si a submonolayer of Ce was deposited by molecular-beam epitaxy (MBE) on the Si substrate. The FET characteristics were found to be much worse for the case without than with IL. From XPS measurements, it was suggested that the oxygen vacancy defects at (near) the CeO_2/Si interface might be the cause of this deterioration in the former case—a somewhat inquieting illustration that a crystalline/crystalline interface may not result in such perfect matching as hoped for, even for a small lattice mismatch as ~0.35% between c-CeO_2 and (111)Si.

As opposed to the latter nominally small lattice mismatch, Klenov *et al.*[32] studied Sc_2O_3 epitaxially grown on (111)Si (mismatch ~10%). Despite the large lattice mismatch, an epitaxial film of Sc_2O_3 with cubic bixbyite structure was obtained with a reaction-layer-free interface as evidenced by HRTEM. These measurements also revealed that the stress, due to the high lattice mismatch was relieved by the formation of a misfit dislocation (MD) network. Besides threading dislocations (TDs), the Sc_2O_3 films were observed to contain a high density of antiphase boundaries (APBs), formed by coalescence of separate film islands, epitaxially nucleating on (111)Si with no unique arrangement of the ordered oxygen vacancies in the bixbyite structure relative to the Si lattice. The authors believe that these APBs are a general feature of the epitaxy of the bixbyite structure (the structure of most RE_2O_3 rare earth oxides) on (111)Si.

B. ESR studies

As previous studies showed, successful epitaxial growth of c-high-κ films on Si is feasible (high quality crystalline films are grown), however, there is evidence that defects located at the interface hamper device performance drastically. To get information about the structure of this interface and defects located at the interface on atomic level, ESR seems a most adequate technique. Also information about defects within the crystalline film can be obtained in this manner.

In the past, the conventional Si/SiO_2 interface has intensively been studied by ESR,[41–44] revealing the paramagnetic P_b-type defects, the dominant interface defect system, identified as trivalent Si centers. These defects, correlating with the crystallinity of the underlying Si substrate face, are inherently incorporated at the Si/SiO_2 interface as a result of the lattice/network mismatch.[45] At the (111)Si/SiO_2 interface, the only type observed—specifically termed P_b, was identified as trivalent interfacial Si (Ref. [41]) ($Si_3 \equiv Si^\bullet$, where the dot represents an unpaired electron in a dangling sp^3 hybrid) backbonded to three Si atoms in the bulk. The technologically favored (100)Si/SiO_2 interface exhibits two types, termed P_{b0} and P_{b1}. The experimental evidence is that P_{b0} is identical to the single P_b defect invariably observed at the (111)Si/SiO_2 interface, but now residing at microscopic interface imperfections. Both, P_b and P_{b0} were, in conjunction with electrical measurements, convincingly established as a main source of electrically detrimental interface defects.[46,47] The P_{b1} center is assigned to a distorted defected

interfacial Si–Si dimer ($Si_3 \equiv Si$—$Si=^\bullet$ defect with an approximately $\langle 211 \rangle$ oriented unpaired Si sp^3 hybrid, where the long hyphen symbolizes a strained bond).[48,49] For standard oxidation temperatures (~850–950 °C) and oxide thicknesses, a density of P_{b0}, $P_{b1} \sim 1 \times 10^{12}$ cm^{-2} each[46] and $P_b \sim 5 \times 10^{12}$ cm^{-2} (Refs. [45], [46], and [50]) is typically observed, respectively, in as-grown (100)Si/SiO_2 and (111)Si/SiO_2, devoid of H passivation.

Another defect of relevance for this work is the EX defect, an SiO_2-associated defect generally observed in Si/SiO_2 entities after thermal treatment.[51–54] The observation of part of the ^{17}O hyperfine structure of EX in ^{17}O enriched (111)Si/SiO_2 structures[55] resulted in the suggestion of a model where EX is depicted as a hole localized over four oxygen DBs formally at the site of a Si vacancy (see Ref. [17] for a brief overview).

Regarding the study on high-κ/Si interfaces, convincing results were obtained by ESR on a-ZrO_2 and a-Al_2O_3 layers grown by atomic layer chemical vapor deposition (ALCVD) on (100)Si substrates,[10] revealing the presence of Si DB-type centers, P_{b0} and P_{b1}. As mentioned above, these defects are the archetypical defects of the Si/SiO_2 interface, so their presence at the high-κ/Si interface would thus herald the presence of a $SiO_{2(x)}$-type IL. Later, similar results were independently obtained on (111)Si/HfO_2 grown by ALCVD and various (100)Si/HfO_2 entities prepared by CVD, and for other high-κ oxides.[11–15] These results point to the formation of a $SiO_{2(x)}$-type IL as endemic for the Si/high-κ metal oxide systems.

However, a recent ESR study[17] has reported, and as so far the sole case, on the ESR-wise absence of these P_b-type centers at a first Si/high-κ insulator interface, i.e., (100)$Si/LaAlO_3$, indicating an abrupt Si/dielectric interface free of an SiO_x IL. So, an $SiO_{2(x)}$ IL-free Si/a-high-κ insulator interface formation appears feasible. Only after annealing at $T_{ox} \sim 800–860$ °C (1 atm $N_2 + 5\%$ O_2 ambient) a Si/SiO_2-type interface starts to form as evidenced by the appearance of P_{b0} defects and EX defects as well. A decrease in P_{b0} defect density upon annealing at $T_{an} \geq 930$ °C indicated that the IL of SiO_2 nature breaks up, which the authors related to $LaAlO_3$ film crystallization and silicate formation.

In the current work, a first ESR study is presented on the atomic nature of inherently occurring (interfacial) point defects in an epitaxial-(high-κ) dielectric/Si structure, i.e., epi-Lu_2O_3/(111)Si with positive lattice mismatch. Measurements in the as-grown state show the epitaxy to be nonperfect, evidenced by the observation of the electrically detrimental P_b interface defects, which are thus revealed and atomically identified as the heralds of imperfect epitaxy. The origin of these P_b defects is suggested to be interfacial Si DBs linked with MDs in epi-insulator/Si systems with *positive* lattice mismatch. The inherent quality and thermal stability as a function of PDA in vacuum (up to ~1100 °C) of the c-Lu_2O_3/(111)Si interface is compared with that of the a-Lu_2O_3/(100)Si one grown in the same MBE system, through monitoring paramagnetic point defects to trace potential fundamental differences. It clearly shows the episystem to have the more stable interface. Initial study on the

electrical deactivation of these defects shows (partial) failure of standard thermal treatments in H_2. Since the P_b traps were shown to constitute a main system of detrimental interface traps in Si/insulator structures, the failing passivation would seriously handicap epitaxial Lu_2O_3 as a candidate for replacement of SiO_2 as gate dielectric in future device generation. Ergo, if this inability to efficiently passivate these interface traps would extend to (positive mismatch) crystalline (high-κ) dielectrics on Si (or other semiconductors) in general, the usefulness of crystalline insulators would be limited throughout.

III. EXPERIMENTAL DETAILS

A. Sample preparation

Epitaxial Lu_2O_3 films (~ 35 nm thick) were grown by reactive MBE on p-type 3 in. (111)Si wafers. The lutetium molecular beam emanated from a Lu charge contained within a tungsten crucible in a high-T effusion cell. Prior to growth, the native SiO_2 on the Si wafers was removed by HF dipping. Once the SiO_2 was removed, the Si wafers were immediately placed into the MBE chamber in which the typical base pressure was $\sim 5 \times 10^{-10}$ Torr. The Si wafers were heated to a substrate temperature (T_{sub}) of 700 °C (measured by an optical pyrometer) and exposed to a lutetium flux in an oxygen background partial O_2 pressure of 2×10^{-8} Torr to deposit epitaxial Lu_2O_3 films at a growth rate of 0.1 Å/s. The films were left uncapped at the completion of growth. Four-circle x-ray diffraction studies showed that the films had the cubic bixbyite structure oriented with the [111] axis along the [111]Si substrate normal, and with the films predominantly (99.8%) grown in the orientation relationship of $(111)[\bar{1}10]Lu_2O_3 \| (111)[\bar{1}01]Si$ (denoted as B-type epitaxy[56]). Rocking curve measurements of the 222 Lu_2O_3 peak revealed a full width at half maximum of 9 arc sec (0.0025°), indicative of a high degree of structural perfection of the Lu_2O_3 films. Scanning transmission electron spectroscopy demonstrated a high quality epitaxial growth, free of any detectable IL. Despite a lattice mismatch f of $\sim 4.5\%$ between Lu_2O_3 and Si, calculated using f $\equiv (2a_{Si}-a_{Lu_2O_3})/a_{Lu_2O_3}$, where a is the lattice parameter, no MDs could be detected in cross-sectional views.[57]

a-Lu_2O_3 films (nominal thickness of ~ 5 nm) were grown on (100)Si wafers in a way identical to the one described above, where the substrates were held at $T_{sub} < 100$ °C in order to form an amorphous layer; the pregrowth thermal flashing was omitted in this case.

B. ESR analysis

An ESR sample was comprised of stacked slices (typically ~ 16) of 2×9 mm^2 main area cut from the wafers with the 9 mm edge along a $\langle 0\bar{1}1 \rangle$ direction, chemically thinned down from the backsides in P etch, which simultaneously eliminates the Si cutting damage (signals). Immediately before every ESR measurement, the sample backsides were carefully selectively etched to remove the oxide. Thermal stability of the grown Si/Lu_2O_3 stacks was analyzed by subjecting the samples to isochronal (~ 10 min) post growth

anneal (PGA) at desired temperatures (T_{an}s) in the range 200–1100 °C in vacuum ($< 4 \times 10^{-6}$ Torr) using a conventional resistively heated laboratory furnace. Generally, separate sets of samples were used for the various thermal steps; some samples were sequentially subjected to multiple PGAs at incremental T_{an}s with ESR diagnosis in between.

Experience with the Si/SiO_2 case tells us that given the ubiquity of hydrogen and its fierce reaction kinetics in point defect passivation through chemical bonding, part of the Si/insulator inherent defect system may be inadvertently left passivated by H (diamagnetic, invisible by ESR), in fact the general case, often overlooked, if not paying particular attention to run H-free processing/and or sample preparation. This was checked, after initial ESR tests, on the as-grown samples by subjection to unbiased vacuum UV (VUV) (=10.02 eV photons, flux $\sim 10^{15}$ cm^{-2} s^{-1}; ~ 10 min–24 h range) irradiation in room ambient prior to next ESR measurement, to maximally reveal all defects through photodissociation of H-terminated DBs.[58] On this matter, VUV has been shown to be most efficient for both oxide (Ref. [59] and references therein) and interface defects (see, e.g., Refs. [10] and [14]), and may additionally unveil nonideal (strained, weak) bonding and activate diamagnetic precursor sites. No effect was observed on the as-grown samples. Yet, over the various postmanufacturing thermal steps carried out, after initial ESR observation the ~ 24 h VUV step was applied routinely to all samples before final ESR measurement. Passivation behavior was analyzed by subjecting a sample to conventional H-passivation in H_2 (99.9999%) at 405 °C for 1 h.

Conventional cw slow passage K-band (20.5 GHz) ESR measurements were carried out at 4.2 K, for the applied magnetic field **B** rotating in the [$0\bar{1}1$] Si substrate plane over an angular range $\Phi_B = 0° - 90°$ with respect to the interface normal **n**, i.e., [100] and [111] for a-Lu_2O_3/(100)Si and c-Lu_2O_3/(111)Si, respectively. Routinely, signal averaging was applied (typically ~ 100 scans) to enhance the signal-to-noise ratio. A comounted Si:P reference sample [g(4.2 K) = 1.99 869 ± 0.00 002] was used for defect (spin) density and g factor calibration. More detail can be found elsewhere.[44,45] To optimize accuracy in defect density determination, the Si:P marker signal as well as sample ESR signals were first simulated based on previously independently acquired knowledge (in particular line shape) about involved signals, i.e., P_b, P_{b0}, P_{b1}, and EX, as described in detail elsewhere.[60] The fitted curves were then individually double numerically integrated and comparatively analyzed. The attained absolute and relative accuracies are estimated at 20% and $\leq 10\%$, respectively.

IV. RESULTS AND ANALYSIS

A. c-Lu_2O_3/(111)Si

An overview of representative first derivative ESR spectra, observed with **B**$\|$[111], the interface normal, on asdeposited c-Lu_2O_3/(111)Si and after different PGA steps is shown in Fig. 1. In the as-deposited state, a single anisotropic signal of small intensity with zero crossing g value $g_c = 2.00 143 ± 0.00 003$ and peak-to-peak width $\Delta B_{pp} = 2.3$ G is observed. Angle dependent measurements for **B**
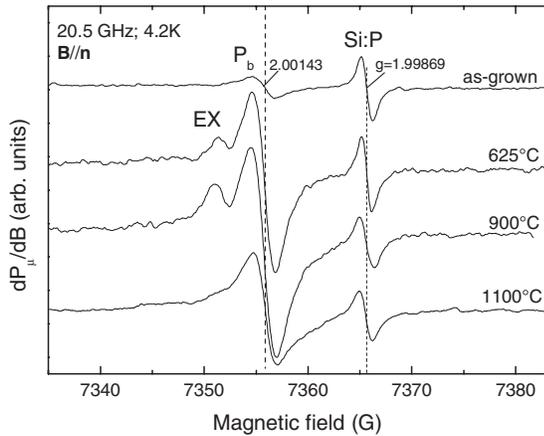
FIG. 1. Representative first derivative-absorption K-band ESR spectra measured at 4.2 K with the applied magnetic field **B** along the [111] interface normal of c-Lu_2O_3/(111)Si structures in the as-grown state and after different PGA treatments in vacuum (10 min) subjected to ~24 h VUV irradiation. Spectra heights have been normalized to equal marker intensity and sample area. The applied microwave power and modulation field amplitude was ~0.8 nW and ~1 G, respectively. The signal at g=1.99 869 stems from a comounted Si:P marker sample.

rotating in the [$0\bar{1}1$] plane led to the single branch g map shown in Fig. 2, pointing to an axial symmetric system with principal g values $g_\parallel$=2.00 143±0.00 003 and $g_\perp$ =2.00 874±0.00 003. These results match the g map of the P_b (Refs. 40 and 45) defect archetypical for the (111)Si/SiO_2 interface, leaving little doubt about the signal's origin. As first straightforward message, it tells us that the epitaxial growth of this Lu_2O_3 film on Si is not perfect. Upon annealing in the range T_{an}~420–550 °C a significant increase in P_b defect density is observed, evidencing the formation of an $SiO_{2(x)}$-type IL. In this temperature range, one more signal appears at g_c=2.00 251±0.00 003, originating from the EX-center, as ascertained by the observation (on optimized spectra—not shown) of the typical copresent hyperfine doublet of ~16.2 G splitting.[51–55] As stated, the EX defect is an SiO_2 associated center, well-known from studies of the Si/SiO_2 structure.[51–55]
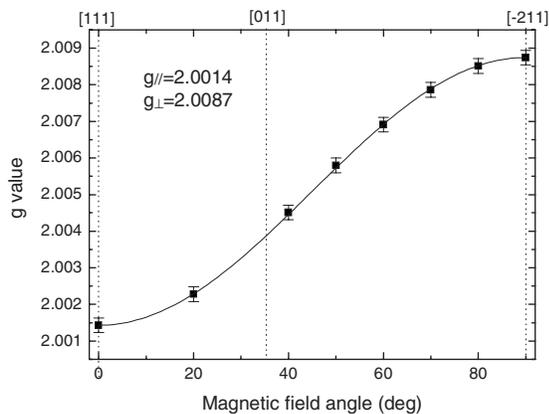

FIG. 2. Angular g map of the observed resonances in c-Lu_2O_3/(111)Si structure for **B** rotating in the [$0\bar{1}1$] plane with respect to the interface normal **n**. The curve represents an optimized fitting of the data for axial symmetry yielding $g_\parallel$=2.00143±0.00003 and $g_\perp$=2.00874±0.00003, found within experimental accuracy to be in agreement with the P_b data for standard thermal (111)Si/SiO_2 structures, confirming the P_b assignment.

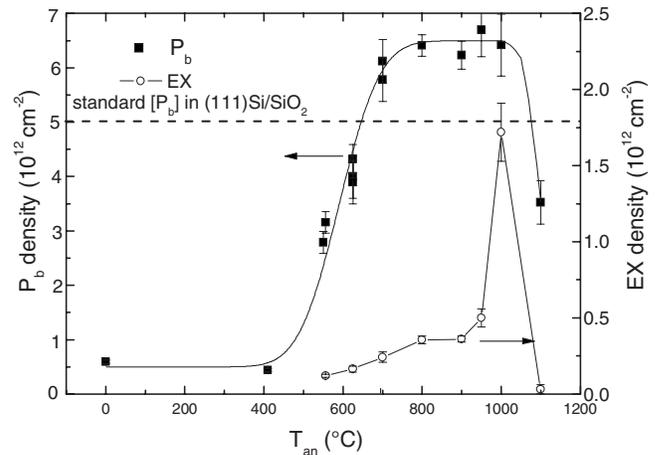FIG. 3. Defect densities, [P_b] and [EX], in c-Lu_2O_3/(111)Si as a function of isochronal (~10 min) PGA treatment in vacuum. The lines are merely meant to guide the eye.

In the as-grown and PGA treated c-Lu_2O_3/(111)Si structures no Lu_2O_3 related paramagnetic point defects could be observed. Neither did supplementary VUV irradiation reveal any Lu_2O_3-associated centers, nor additional P_b defects, indicating there apparently being no inadvertent H passivation involved, as expected from the applied nominally H-free MBE sample growth.

The main PGA results are compiled in Fig. 3, showing the inferred density of the observed defects as a function of PGA temperature on VUV-treated samples. Different aspects are worth mentioning.

In the as-grown state, a P_b density of (5.9±0.4) ×10^{11} cm^{-2} is found, corresponding to approximately one tenth of the value (5×10^{12} cm^{-2}) inherent to[45,46,50] standard thermal (111)Si/SiO_2 grown in the range 850–1000 °C (see dashed horizontal line in Fig. 3). This provides, on atomic scale, direct evidence of interfacial defects at this epitaxial interface. But the interface thus still appears inherently about ten times better than standard thermal (111)Si/SiO_2, a noteworthy aspect indeed. Yet, in taking a contrary view, one might blame the P_b appearance to putative $SiO_{2(x)}$ IL formation, but then it would indicate, at least, that no full sample wide SiO_2-like IL has formed. The width ΔB_{pp}~2.3 G of the current P_b signal is somewhat larger than that (~1.3 G) observed for standard thermal (111)Si/SiO_2 interfaces grown at ~970 °C.[45,61] It points to a somewhat increased amount of strain at the interface,[44,45,62,63] where the higher level of stress at the origin can be explained by the large mismatch between c-Lu_2O_3 and Si (~4.5%). This low density of interface defects is retained under subsequent PGA treatments up to T_{an}~420 °C.

Upon annealing from T_{an} ~420 °C onward, the structure becomes thermally unstable as indicated by the steadily growing P_b density up till $T_{an}\approx700$ °C to reach [P_b] ~6.3 ×10^{12} cm^{-2}, a density comparable, yet ~30% higher, than the natural occurring density in thermal (111)Si/SiO_2. It would indicate that the epi-Lu_2O_3/(111)Si interface has transformed into truly Si/$SiO_{2(x)}$-type, evidencing formation of an $SiO_{2(x)}$-type IL. This formation of an Si/SiO_x-type interface may be put in the light of such previously observed

IL formation in the a-LaAlO$_3$/(100)Si system, linked with the transformation of the LaAlO$_3$ network from the amorphous to the polycrystalline state.[17] Following subsequent annealing at higher T_{an} up to $\sim$1000 °C, that situation does not change as [P$_b$] remains constant. Here, it may be added that SiO$_{2(x)}$-type IL formation after PGA at 400 °C (1 Torr O$_2$) in the case of amorphous-Lu$_2$O$_3$/(100)Si entities has been concluded from x-ray electron spectroscopy.[16]

The gradual growth from $T_{an} \approx 420$ °C onward of an Si/SiO$_2$-type interface is independently affirmed (see Fig. 1) by the observation, after VUV irradiation, of the SiO$_{2(x)}$ associated EX defect.[51–55] It starts being observed at T_{an} $\sim$550 °C and increases to the density of $\sim$4$\times$10^{11} cm^{-2} after annealing at 800 °C; like P$_b$, its areal density remains rather unchanged up to T_{an}=950 °C. The growth temperature profile of EX appears upward shifted (retarded over $\sim$100 °C) compared to P$_b$, indicating an additional growth (or modification) of the IL. No information on the IL thickness was obtained. For still higher T_{an} ($>$1000 °C), both defect densities in tandem drop drastically, indicating the Si/SiO$_2$-type interface to collapse, i.e., elimination of the "pure" SiO$_x$ component. This disruption of the interface, i.e., the breaking up of the SiO$_x$-IL, is possibly linked to the previously observed[25] decomposition (metallic Lu formation) of the ALD Lu$_2$O$_3$ layer of a-Lu$_2$O$_3$ (2–5 nm)/Si structures.

It is our main interest to study the *intrinsic* density of defects located at or near the c-Lu$_2$O$_3$/(111)Si interface. Therefore, one should ensure that no defects are left inactivated (passivated by H), that is, invisible for ESR. Thus, different depassivation tests, using VUV irradiation ($\sim$10 eV) to remove H from possibly passivated defects, were performed on the as-deposited sample as well as on the samples vacuum annealed at 625 and 950 °C ($\sim$10 min). To enhance confidence (VUV irradiation approach to the interface) the Lu$_2$O$_3$ layer of an as-deposited sample was first thinned down through chemical etching to a thickness of 9 $\pm$ 1 nm, as measured by spectroscopic ellipsometry. Comparative ESR analysis before and after VUV treatment for different times (10 min–24 h range) found no difference in P$_b$ density. To probe further, the VUV tests were repeated on the same samples after degradation treatment, i.e., enhanced Si/SiO$_2$-type interface formation through vacuum annealing at 650 and 950 °C, leading to substantial densities of P$_b$ centers (see Fig. 3) which were subsequently efficiently passivated by H through the usual annealing in H$_2$ at 405 °C (see next paragraph). Now, the interfacial P$_b$ centers were found to be gradually ESR (re)activate under continued VUV irradiation, herewith clearly bearing out the efficiency of VUV treatment. This all indicates that the defect densities measured here on as-received samples and after vacuum annealing represent the intrinsic density of interface defects, without any noticeable inadvertent H passivation interfering, as might be expected from the nominally H-free epi-Lu$_2$O$_3$ layer growth by the MBE method.

Traps located right at the dielectric/Si interface are disastrous for MOS device performance, so these should be suppressed inherently, or if occurring, efficiently inactivated. Although the conventional device structure (100)Si/SiO$_2$, in-
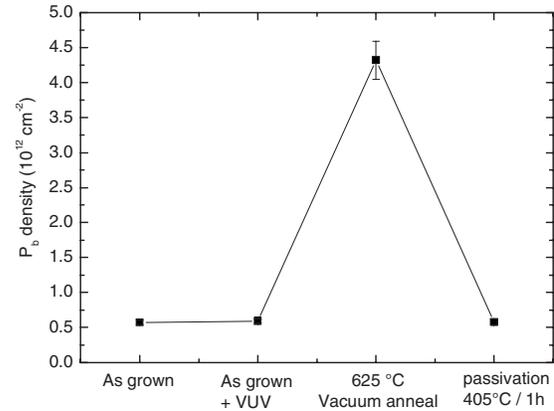

FIG. 4. Measured P$_b$ defect density in c-Lu$_2$O$_3$/(111)Si as a function of different sequential post deposition treatments. The lines guide the eye.

variably, exhibits an inherent density of P$_{b0}$ interface traps of $\sim$1$\times$10^{12} cm^{-2}, the unprecedented success of this structure in the device world owes much to the fact that these traps can be efficiently inactivated down to the (sub) 10^{10} cm^{-2} eV^{-1} level through binding with (passivation by) hydrogen, readily achieved by a standard anneal treatment ($\sim$420 °C; 1 h) in H$_2$-rich ambient—industrially, anneal in forming gas (10% H$_2$ in N$_2$). In the current case of c-Lu$_2$O$_3$/(111)Si, we find an inherent density of interface traps [P$_b$] $\sim$5.9 $\times$10^{11} cm^{-2}, still not device grade to start with, but already being substantially and promisingly smaller than the inherent density in conventional (100)Si/SiO$_2$. After annealing at $T_{an} > 500$ °C this density increases, so the question arises if the usual standard H-passivation treatment would be able to deactivate these interface traps as efficiently as it would do for the standard Si/SiO$_2$ structure. This was tested on a set of c-Lu$_2$O$_3$/(111)Si samples, annealed in vacuum at 625 °C for 10 min, which after first ESR measurement was subjected to standard treatment in pure H$_2$ (405 °C, $\sim$1 h) and then remeasured by ESR. The results are summarized in Fig. 4. Disquietingly, it is found that in the passivated sample, a P$_b$ density of (5.8 $\pm$ 0.6)$\times$10^{11} cm^{-2} remains, i.e., the standard H-passivation procedure appears to fail to deactivate these fast interface traps below the 10^{11} cm^{-2} eV^{-1} level. A similar test carried out on a sample with the epi-Lu$_2$O$_3$ layer thinned down (5 $\pm$ 1 nm) led to identical results, making any hydrogen diffusion limitation influence improbable. Remarkably, the density of P$_b$ defects left active equals, within experimental uncertainty, the one observed in the as-grown state, i.e., the signal observed in the as-grown state might arise from the same set of defects which then, apparently, cannot be passivated.

Passivation in H$_2$ experiments were also conducted on samples subjected to 950 °C vacuum anneal degradation treatment, resulting in "full" Si/SiO$_2$-type interface formation in terms of observed P$_b$ centers. Now, by contrast, treatment in H$_2$ is found to efficiently passivate P$_b$ centers down to the sub ESR detection limit ($\sim$1$\times$10^{11} cm^{-2}). In support of previous inference, it would indicate that he epi-Lu$_2$O$_3$/(111)Si interface with presumed incorporation of detrimental MDs has been transplanted by a "conventional"
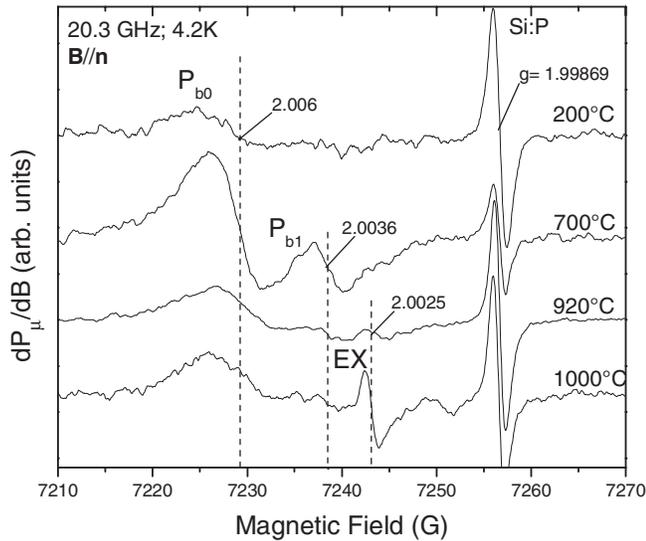
FIG. 5. K-band ESR spectra measured at 4.2 K with **B** along the interface normal [100] of a-Lu$_2$O$_3$/(100)Si structures after different isochronal (~10 min) PGA treatment in vacuum. Spectra heights have been normalized to equal marker intensity and sample area. The applied microwave power and modulation field amplitude was ~0.5 nW and ~1 G, respectively.

FIG. 6. Observed densities of P$_{b0}$, P$_{b1}$, and EX defects in a-Lu$_2$O$_3$/(100)Si as a function of the PGA treatment temperature in vacuum, followed by 24 VUV irradiation. The bold dashed horizontal line marks the inherent, about equal, density of P$_{b0}$ and P$_{b1}$ interface defects in standard thermal (100)Si/SiO$_2$ grown in the range 800–960 °C. The thin dotted curve guides the eye.

a-SiO$_2$/(111)Si interface, where likely some interfacial Si layers have been oxidized with attendant MD effect elimination.

B. a-Lu$_2$O$_3$/(100)Si

Figure 5 presents an overview of ESR spectra observed for **B**∥**n**, on an a-Lu$_2$O$_3$/(100)Si structure after different PGA treatments in vacuum. No successful measurement could be done on the as-deposited sample due to poor signal-to-noise ratio. After annealing at 200 °C, an anisotropic signal of g$_c$=2.0060±0.0002 and ΔB$_{pp}$~7.5 G was observed. Angle dependent measurements for **B** rotating in the [0$\bar{1}$1] plane revealed an axial symmetric system with principle g values g$_∥$=2.00 185±0.00 003 and g$_⊥$=2.00 855±0.00 003, matching the g map of the archetypal P$_{b0}$ (Ref. 44) interface defect in thermal (100)Si/SiO$_2$ interface, thus identifying the defect. Upon annealing at 570 °C one more anisotropic signal appears with g$_c$=2.0036±0.0002 and ΔB$_{pp}$~4.3 G, of which additional mapping convincingly showed it to concern the P$_{b1}$ defect, the second archetypical interface defect for the (100)Si/SiO$_2$ interface. After annealing the structure at 920 °C a third, now isotropic, signal was observed in increasing intensity, stemming from the EX defects, as evidenced by the observation of the copresent characteristic hyperfine splitting of ~16.2 G. No Lu$_2$O$_3$-related paramagnetic point defects could be observed.

An overview of all PGA results is compiled in Fig. 6, showing the density of observed defects as a function of PGA temperature. Already after 200 °C vacuum anneal a P$_{b0}$ defect density of (2.6±0.5)×10^{12} cm^{-2} is observed—clear evidence for the presence of an the SiO$_x$ IL. This density of interface traps is already 2.5 times higher than observed in standard (100)Si/SiO$_2$ (see horizontal dashed line in Fig. 6) indicating that the interface between the SiO$_2$ and Si in the a-Lu$_2$O$_3$/(100)Si entity is of inferior electrical quality. An-
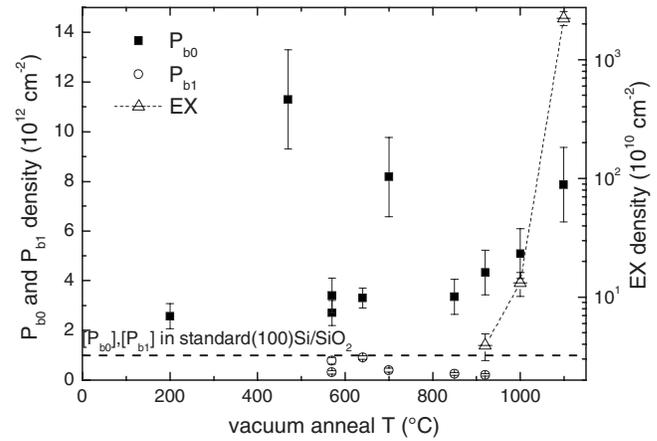
nealing the samples to higher temperatures results in different fluctuating densities of P$_b$ defects, suggesting an unstable interface. No general trend in interface trap density upon PGA could be found. After PGA at 570 °C a weak P$_{b1}$ signal appears, with density ~5×10^{11} cm^{-2}, which may be compared with the inherent value[46] [P$_{b1}$] ~1×10^{12} cm^{-2} for standard thermal (100)Si/SiO$_2$. For higher T$_{an}$, the signal weakens. The absence of the P$_{b1}$ defect at lower T$_{an}$ may be understood on grounds of general (100)Si/SiO$_2$ properties bearing out that ESR-active P$_{b1}$ defect formation requires some minimal thermal budget.[64] The SiO$_x$-associated EX defect appears from T$_{an}$~920 °C onward, independently evidencing of the presence of a SiO$_x$-type IL.

Altogether, the a-Lu$_2$O$_3$/(100)Si interface emerges as an unstable interface with the presence of an SiO$_x$-IL with inferior (electrical) interface properties.

In a similar way as done for the case of epitaxial c-Lu$_2$O$_3$ layers, the efficiency of passivation treatment in H$_2$ has also been analyzed for a-Lu$_2$O$_3$ films. This was carried out on a set of a-Lu$_2$O$_3$/(100)Si samples first subjected to vacuum annealing (640 °C; 10 min), exhibiting defect densities [P$_{b0}$]=(3.3±0.2)×10^{12} cm^{-2} and [P$_{b1}$] ~0.9 ×10^{12} cm^{-2}. Quite in contrast with the epi-Lu$_2$O$_3$ case, subsequent passivation treatment in H$_2$ (405 °C; 1 h) was found to eliminate the defects below the detection limit (density <1×10^{11} cm^{-2}), indicating a similar efficiency of the H$_2$ treatment as for the conventional a-SiO$_2$/(100)Si structure. It points to a Si/SiO$_2$ nature of the interface, in agreement with previous inferences.

V. DISCUSSION

A. epi-Lu$_2$O$_3$/(111)Si

1. As-grown epi-Lu$_2$O$_3$/(111)Si

Touching the basic physics of heteroepitaxy, without doubt, the most fundamental question abounding concerns the origin and incorporation in the interfacial morphology of the revealed P$_{b0}$ centers at the epi-Lu$_2$O$_3$/(111)Si interface,

pointing to imperfect epigrowth—in fact, the defects appearing as inherent relicts of such growth. Entering into this, as a preamble general note, interfacial point defect appearance may perhaps not come as a surprise at all given the rather substantial mismatch in lattice parameters between the matching epifaces of the Lu_2O_3 and Si crystals. We may envisage several possibilities.

First, it would seem natural to start from the involved mismatch of ~4.5% between Lu_2O_3 and Si in this heteroepitaxial growth. As known, when the pseudomorphic film thickness exceeds a critical thickness d_c, the film will plastically deform (relax) through the formation of a MD network. The value of d_c may be obtained from the equation $d_c \approx b/(6f)$, a rough approximation of the transcendent theoretical result[65]

$$d_c = \frac{b}{8\pi f(1-\nu)}\ln\left(\frac{ed_c}{r_0}\right),$$

obtained within the force balance model (balance between plastic deformation force and shear stress), where b is the dislocation Burger vector, ν the Poisson ratio, $f=\Delta a/a$ the lattice parameter (a) mismatch, r_0 the core radius of the dislocations, and $e=2.7183$. For the current case, with f ~4.5% and using $b=0.38$ nm typical for Si, we obtain an upper limit $d_c \sim 1.4$ nm $\ll d_{Lu_2O_3} \sim 35$ nm of the grown Lu_2O_3 epifilm. Thus a MD network should have formed, although no such MD network could be directly demonstrated in cross-sectional scanning trasmission electron spectroscopy (STEM) views; it might indicate the film not to be totally relaxed. So, in a first picture, one may surmise that, in view of the ~4.5% lattice mismatch between Lu_2O_3 and Si, the occurring P_b defects arise as intrinsically connected with introduced MDs, e.g., an hexagonal network of MDs parallel to $\langle 11\bar{2}\rangle$ Si, as reported for the isomorphic epi-Sc_2O_3/(111)Si structure, grown with the orientational relationship described by $[111]Sc_2O_3 \| [111]_{Si}$ and $(1\bar{1}0)Sc_2O_3 \| (1\bar{1}0)_{Si}$.[32] Should no reconstruction occur in the MD core, the MDs would constitute rows of ordered Si DBs at the (111)Si/dielectric interface all potentially appearing as P_b-like centers. Indeed, paramagnetic Si DB-type defects related to deformation induced dislocations in bulk Si have been reported by ESR observations, referred to as Si–R or D centers observed at $g=2.005$ after annealing at $T \geq 800$ °C.[66] Now for f ~4.5%, and assuming a fully relaxed Lu_2O_3 epifilm (nonpseudomorphic), this would result in a MD network involving ~3.5×10^{13} cm^{-2} defected interfacial Si atoms, that is, the same number of Si DBs if no core reconstructuring would occur, about 60 times larger than the detected P_bs for the sample in the as-grown state. So, on this account the observed P_bs could well be related with MDs; yet according to ESR observations for bulk dislocations on Si,[66,67] distinct bond reconstructuring should have occurred. The latter is also corroborated by current ESR spectral properties: If P_bs would occur as (maximally) densely ordered along dislocation line edges, it would give rise to explicit dipolar fine structure in this ordered two-dimensional spin system [dipolar interaction of a central P_b with a 4th neighbor P_b spin results in a fine structure doublet of ~7.7 G (Ref. 68)],

which is not observed. Despite the limited ESR sensitivity, this together with the absence of excessive dipolar line broadening, would indicate no substantial P_bs occurring within the 4th–5th neighbor position range along the dislocation lines. So, all in all, within the scope of available data (defect densities), the relationship of P_bs with MDs is feasible. Importantly, in this view and assuming a truly abrupt interface, it would indicate the P_b defect able to occur at a Si/insulator interface in no strict Si/SiO$_2$-type environment.

A second view might envision imperfect epitaxy. As P_b is an interface defect archetypal for (111)Si/SiO$_2$, its occurrence could indicate some nonuniform epitaxy, in that some small irregular patches of SiO$_2$ IL could have formed. Here, if a standard type 700 °C thermal (111)Si/SiO$_2$ interface would have formed, the patches should exhibit an inherent P_b density of ~5×10^{12} cm^{-2}. Then an observed density of ~5.9×10^{11} cm^{-2} in the as-grown state would indicate the Si/SiO$_2$ patch area to make up ~12% of the total Si/dielectric interface area—probably unacceaptably unrealistic for a successful pseudomorphic epilayer growth. Another result that would counter this interpretation comes from post-manufacturing passivation heat treatments in H$_2$. Here, it was observed that passivation treatment in H$_2$ (1 atm; 1 h; 405 °C) still left a remaining density $[P_b] \sim 5.8 \times 10^{11}$ cm^{-2}, i.e., still about the density encountered in the as-grown epistate. It indicates that the P_b defect system cannot be inactivated below the initial density, which behavior would be rather unexpected for conventional (111)Si/SiO$_2$ areas where P_bs can be readily passivated by such treatment to well below the ESR detection limit (few times 10^{10} cm^{-2}).

As third possible origin of the P_b signal one could consider a variant on the first one. Point defects could originate from planar interface defects called APBs (Ref. 32) and related TDs at APB triple junctions. The bixbyite structure of c-Lu_2O_3 can be described as a vacancy-ordered fluorite with two oxygen vacancies per unit cell. When islands of the c-Lu_2O_3 bixbyite structure nucleate on Si, they have inherently no uniquely preferred arrangement of these ordered oxygen vacancies relative to the Si surface. When two islands that have their oxygen vacancy sublattices shifted relative to each other coalescence, APBs are expected to form. These APBs were experimentally observed by HRTEM on Sc_2O_3/(111)Si structures[32] and, as stated before, are believed to be a common feature of the epitaxy of bixbyite structure films on Si. Clearly, these ABPs and related TDs are predominantly a matter of imperfections within the epitaxial bixbyite Lu_2O_3 film. Within the current context, what then only could matter potentially is what kind of "defect imprint" these would leave at the Si/Lu_2O_3 interface, i.e., where APBs meet the Si interface, Si DBs, possibly appearing as ESR-active P_b centers, may arise. Though their relevance to the occurring P_b system is considered second to that of the MD network at the Si substrate face, their contribution cannot be excluded; only growth of monocrystalline epilayers could resolve this.

Finally, starting from the view of perfect epitaxial growth, as a fourth possibility, one could suggest the incorporated P_b defect system to stem from unavoidable steps at the pristine initial Si surface[37] impairing perfect epitaxial in-

terface registry anyway. However, in a straightforward (ball-and-stick) picture, arguably, such step edges (1–3 atom steps) at the (111)Si surface would naturally lead to 19°-type P_b variants,[69] i.e., with the unpaired Si sp^3 hybrid along the crystallographically equivalent [111] directions at ~19° with the (111) surface rather than the observed regular 90° P_b centers. So, this possibility seems countered on ESR basis.

Taken altogether, the above considerations lead us to the suggestion the observed P_bs in as-grown epi-Lu_2O_3/(111)Si entities to be related to MDs, considered as unavoidably incorporated to account for the 4.5% lattice mismatch. Here, we also want to add that Lu_2O_3 has the highest mismatch of any RE oxides on Si. In that sense, the current work is a worst case study and it would thus be of much interest to study, e.g., epi-Gd_2O_3/Si which is approximately ten times better lattice matched than Lu_2O_3/Si, to verify current findings and conclusions. According to current results, epi-Gd_2O_3/Si would provide a better interface in terms of the occurrence of inherent detrimental P_b-type defects.

2. Thermal stability

A main impetus to the exploration on the use of high-κ materials in crystalline form is to provide a fundamental solution to unwanted (SiO_x) IL formation through exact crystallographic matching at the semiconductor/insulator interface creating, ideally, a "zero" defect interface. But of course, once created, at least as important is that the structure must additionally prove thermodynamically stable to maintain the superb interface quality during necessary device fabrication thermal steps. It makes thermal stability analysis a key point, also addressed here.

In the as-grown state, the c-Lu_2O_3/(111)Si interface starts off as a good interface with a relatively low interface trap density, i.e., ~10% of that in standard (111)Si/SiO_2. However, already after a PGA in vacuum at ~550 °C an SiO_x IL starts to form, which of course, when happening, results in the loss of the potential advantages related with the use of crystalline high-κ's on Si. After a PGA at 700 °C a "full" $SiO_{2(x)}$ layer is grown with an intrinsic interface defect density even surmounting that of standard thermal (111)Si/SiO_2. This may result from the increased stress located at the Lu_2O_3/(111)Si interface due to lattice mismatch. Since in device fabrication, the dielectric material is deposited in the middle of the process sequence with multiple high-T (>500 °C) steps applied afterwards, the use of crystalline high-κ layers, in the case of Lu_2O_3 at least, would provide no advantage over a-insulators.

As prospected by ESR, the thus far best amorphous high-κ/Si interface in terms of interface defects is definitely $LaAlO_3$/(100)Si.[17] In as-grown a-$LaAlO_3$/(100)Si no paramagnetic interface defects (P_{b0} and P_{b1}) could be observed, i.e., $[P_{b0}] \leq 1 \times 10^{10}$ cm^{-2}. Comparison with the current results tells us that in terms of detrimental interface traps the c-Lu_2O_3/(111)Si interface is of inferior quality compared to the a-$LaAlO_3$/(100)Si one. This latter defect-free interface is maintained up to PGA at 800 °C before an SiO_x IL starts to form, whereas the c-Lu_2O_3/(111)Si structure already shows evidence of an SiO_x IL after PGA at 550 °C. Pertinently, to

this should be added that PGAs in the case of a-$LaAlO_3$/(100)Si are even performed in O_2 rich (5% O_2 in N_2) ambient versus vacuum ($\leq 4 \times 10^{-6}$ Torr) for the current study on c-Lu_2O_3/(111)Si. The latter would thus clearly fall short in thermal stability.

But here we should remark that this apparent inferior stability of the Lu_2O_3/Si structure may only be seeming: As interfacial Si will like to oxidize if reached by oxygen, we should note that Lu_2O_3 has a much higher oxygen diffusion coefficient than $LaAlO_3$, basically because 1/4 of the oxygen sites in the fluorite structure are empty to make it into a bixbyite. So, during PD thermal treatment in a vacuum ($\leq 4 \times 10^{-6}$ Torr) with insufficiently reduced partial O_2 pressure (p_{O_2}), the formation of interfacial SiO_x even at far lower temperatures may not come as a surprise. At such p_{O_2} values, interfacial SiO_x layers may readily form over periods of minutes. Rather, the fact that an abrupt interface between epitaxial Lu_2O_3 and Si can be grown at 700 °C would just indicate that the Lu_2O_3/(111)Si interface is thermodynamically stable. Then, what the current result would indicate is that the MBE-grown c-Lu_2O_3/(111)Si structure would not meet current technological demands if lacking control over unwanted interface-degrading oxygen penetration. Under such constellation, it is obvious as well why epitaxially grown high-κ layers will provide no advantage over a-insulators.

A PGA treatment at $T_{an} > 1000$ °C results in the disintegration of the interface for both a-Lu_2O_3/Si and c-Lu_2O_3/Si structures.

3. Passivation behavior

The technologically favored (100)Si/SiO_2 interface has inherently an interface defect density of $[P_{b0}] \sim 1 \times 10^{12}$ cm^{-2}. This would actually be a useless interface in terms of detrimental interface traps of it were not that a simple treatment in H_2-rich ambient (400 °C, 1 h) is able to deactivate these traps to the (sub) 10^{10} cm^{-2} eV^{-1} level, creating the superb interfacial quality of (100)Si/SiO_2 used in devices. In the present case, the c-Lu_2O_3/(111)Si structure has an inherent interface defect density of $[P_b] \sim 5.9 \times 10^{11}$ cm^{-2}, which would thus constitute a better starting position than standard (100)Si/SiO_2. Yet, after subjecting a vacuum annealed (625 °C) c-Lu_2O_3/(111)Si structure, with enhanced P_b density, to a similar H-treatment (405 °C, H_2, 1 h) a P_b density of ~5.8×10^{11} cm^{-2} remains, i.e., these detrimental interface traps cannot be deactivated by standard H-treatment. This high level of left active traps located right at the interface will out rightly render the c-Lu_2O_3/(111)Si device unfit. This behavior contrasts with that of Lu_2O_3 films deposited amorphously on (100)Si, where the usual H_2 passivation treatment is found to work properly, similar to the standard a-SiO_2/(100)Si case. This has been ascribed to the overall Si/a-SiO_2 nature of the interface with correlated flexibility of the amorphous structure to adapt, with attendant reduction in stress, to the mismatch brought about by a crystalline surface. It would thus rather concern a conventional-like Si/$SiO_{2(x)}$ interface case, where the mismatch is accounted for by a number of randomly distributed interface defects with known H passivation properties.

We may understand the failing passivation efficiency in the epi-Lu_2O_3 case. As hinted at above, the ESR active P_b defects remaining after H-treatment probably come from interface regions with high levels of stress, such as MDs and, possibly, APB's. At least the first type of these line defects are believed to be a general feature of epitaxial growth of high-κ oxides on Si; APBs, in principle, can be avoided by growing monocrystalline epilayers. Such regions of enhanced local strain[66,70] are expected to be accompanied by substantially *enlarged* spreads σ_{Ef} and σ_{Ed} in the Arrhenius-type activation energies E_f and E_d for the chemical reactions of P_b passivation in H_2 and P_bH dissociation, respectively.[71] Within the gained insight[71] on P_b-hydrogen interaction kinetics, the simultaneous action of passivation and dissociation reactions makes this to result in increasing degradation of P_b passivation efficiency. Along straightforward analysis,[71] for the applied passivation temperature of ~405 °C, the occurrence of relative spreads $\sigma_{Ef}/E_f = \sigma_{Ed}/E_d \sim 9-16\%$, that is, $3-4\times$ enhanced compared to those for standard thermal $(111)Si/SiO_2$ grown in the range $850-950$ °C, would prevent reduction of $[P_b]$ below 5×10^{11} cm^{-2}. While uncommon for standard $(111)Si/SiO_2$, it is well feasible for the situation of MDs, constituting regions of substantially enhanced strain.[66,70] Possibly some improvements here could be obtained by resorting to enhanced H_2 pressure or somewhat higher H_2 treatment temperature (~480 °C).

This would imply that, if P_b's located at these line defects would exhibit the general disastrous property of resisting passivation in H_2, MDs have to be avoided, which will drastically limit the usefulness of crystalline high-κ oxides as gate insulators in general. Through the inherently related point defects, the interfacial edge component containing MDs would thus emerge as an interface killing item in epi-insulator/Si heterostructures. In this view, only crystalline high-κ oxides with a high, ideally perfect, degree of lattice matching to the substrate could be used, or else, restrict epilayer thickness to below d_c. To be clear, the finding of the detrimental influence of MDs on semiconductor heterostructures is not surprising; it is broadly known from other fields, such as optoelectronics. In fact, unavoidable MD formation constitutes the mere reason why many "obvious" device fit structures cannot be realized at all. What the current work importantly exposes is that MDs, at least for the epi-insulator/Si case, entail electrically detrimental point defects, identified as P_b-type centers, that resist to efficient passivation by hydrogen.

4. Device grade epitaxial insulators

On the basis of the current data, establishing of device grade epi-insulator/Si (semiconductor) entities would in essence leave only two choices: (1) selecting epi-insulator/c-Si systems of favorably low mismatch f, so as to keep intrinsic MD-associated point defects below critical levels; (2) restricting epilayer growth to subcritical thickness, e.g., ≤1.4 nm for f$\sim4.5\%$ as in the current case. Device wise, this would not constitute much of a problem in principle, but as to the epi-insulator/Si interface, there will be an additional impact, potentially either beneficial or detrimental, of the necessary gate contact layer to be put on. But clearly, more

ESR studies on different types of epitaxial high-κ's on Si with different lattice mismatch are needed to verify the generality of this conclusion.

We may put the current findings in the light of previous results. A high-κ material with a small lattice mismatch with the Si crystal is CeO_2 (mismatch with $(111)Si\sim0.35\%$). As mentioned, Nishikawa *et al.*[36] investigating $CeO_2/(111)Si$ entities found that the quality of MISFETs made with c-CeO_2 directly grown on $(111)Si$ was inferior to the one made with a deliberate IL. This degradation was due to a larger density of interface states, detected by the charge pumping method, and was attributed to a large number of oxygen vacancy defects at the c-$CeO_2/(111)Si$ interface. Interpretating these results within the framework of the current work, the defects located at the $CeO_2/(111)Si$ interface, which degrade the device performance, may be instead P_b-type defects located at MDs. This would indicate that even for reduced lattice mismatch, the electrically detrimental P_b defects may remain an ultimate threat for the crystalline high-κ insulator/Si interface if effective passivation fails. In this view, the suitability of crystalline high-κ dielectrics in future device fabrication may appear limited, its usefulness likely being predominantly determined by the level of natural interface mismatch.

B. Comparison between c- and a-Lu_2O_3 layers

Here, to start with, it needs to be mentioned that the comparison between epi- and a-Lu_2O_3 layers regarding the inherent quality and the thermal stability of the interfaces made with Si is made between c-$Lu_2O_3/(111)Si$ and a-$Lu_2O_3/(100)Si$, that is, dissimilar c-Si faces, yet it is felt still valid conclusions can be drawn: Partly by comparing the properties of occurring point defects, such as P_b-type centers, on relative basis with those of the respectively isoface $SiO_2/(111)Si$ and $SiO_2/(100)Si$ interface ones, and second, overall major thermal interfacial interactions (chemical, diffusion) will occur comparable, whatever the initial interfacial c-Si faces.

Comparing Figs. 3 and 6, we observe that in the as-grown state, the inherent density of interface traps (P_b-type centers) in c-$Lu_2O_3/(111)Si$ is approximately ten times smaller than in standard thermal a-$SiO_2/(111)Si$, while, by contrast, the a-$Lu_2O_3/(100)Si$ interface is at least two times worse than the superb a-$SiO_2/(100)Si$ interface. The latter may not come as a surprise since it concerns a low T(<100 °C) grown Si/SiO_2 interface.[64] So, on this relative basis, the epigrowth out performs the a-Lu_2O_3 growth over 20 times —a drastic difference indeed.

Differences in the thermal stability are noted as well. A first major one appears the overall defect density evolution versus T_{an}. Starting off with an interface of reasonable quality in terms of occurring P_b centers (Fig. 3), the c-$Lu_2O_3/(111)Si$ interface keeps that quality up to ~420 °C, from where it develops in a monotonous way toward a close-to-standard a-$SiO_2/(111)Si$ interface to maintain this for T_{an} up to ~1000 °C. The a-$Lu_2O_3/(100)Si$ system, by contrast, while never reaching a state of improved interface quality (in terms of P_b centers) compared to the

a-SiO$_2$/(100)Si reference, shows a somewhat confused thermal instability reflected by the fluctuation in [P$_b$] (Fig. 6). Yet, with the general trend of increasing [P$_{b0}$] with growing T$_{an}$, it points to an unstable, worsening system. This means that in terms of inherent interface quality the c-Lu$_2$O$_3$/(111)Si is superior to the a-Lu$_2$O$_3$/(100)Si structure. Perhaps, the sole common trend for both systems is increase in P$_b$-type defect density from T$_{an} \geq 460$ °C onward.

As to a-Lu$_2$O$_3$/(100)Si, one additional noteworthy aspect concerns the P$_{b1}$ center. It only appears after annealing at T$_{an} \sim 570$ °C, in substandard a-SiO$_2$/(100)Si density, to fade with increasing T$_{an}$. As outlined previously, like P$_{b(0)}$, the P$_{b1}$ center also entails an unpaired sp^3 hybrid at an interfacial threefold Si atom, seen as part of a defected strained Si–Si dimer ($\equiv$Si–Si$^\bullet$=Si$_2$), thus basically of the same chemical identity as P$_{b(0)}$, yet physically different, e.g., regarding hybrid orientation, bond strain and structural relaxation.[48,49] Generally, P$_{b0}$ and P$_{b1}$ centers are mostly observed in tandem at the a-SiO$_2$/(100)Si interface, although relative intensities may vary. Along that criterion, in line with previous inferences, the ESR results also indicate a conventional-like (100)Si/SiO$_{2(x)}$ interface formation in the nominally a-Lu$_2$O$_3$/(100)Si system from T$_{an} \sim 570$ °C onward. Yet, nonstandard P$_{b1}$ behavior, in fact, plain absence of a P$_{b1}$ signal for T$_{an} < \sim 570$ °C, was also noticed in the ESR-probed thermal evolution of the LaAlO$_3$/(100)Si structure grown by MB deposition.[17] One possible reason advanced there was insufficient interface (oxide) relaxation, i.e., not attaining a minimum level required for P$_{b1}$ formation,[64] as generally inherently established during uncomplexed oxidation of Si at high-T in O$_2$.

Finally, as already discussed at length, there is the striking difference between the epi- and a-Lu$_2$O$_3$ cases in regard to the efficiency of achievable passivation of interfacial P$_b$ traps, i.e., attainable level of inactivation by standard passivation treatment in H$_2$. Here, while the as-grown epi-Lu$_2$O$_3$/Si system would be at the loosing end, that inequality will be entirely eradicated after device manufacturing thermal steps. So, on this matter, both types of interfaces would end on equal level.

VI. SUMMARY AND CONCLUSIONS

We have reported on a first ESR analysis of inherently occurring point defects in an epitaxially grown high-κ insulator/c-Si structure, i.e., c-Lu$_2$O$_3$/(111)Si, with special attention to the crystalline interface in terms of occurring paramagnetic point defects. Samples were analyzed in the as-grown state, after PDA treatments at different temperatures in vacuum for 10 min, and after standard H$_2$-treatment (405 °C, H$_2$) in order to deactivate interface traps. Finally, a comparison of inherent quality and thermal stability of the interface was made between c-Lu$_2$O$_3$/(111)Si and a-Lu$_2$O$_3$/(100)Si.

The ESR analysis leads to noteworthy findings: (1) in the as-grown state, P$_b$-type defects (the archetypal defects at the (111)Si/SiO$_2$ interface) are observed, indicative of a nonperfect epitaxy. The origin of the defects, constituting a major system of electrically detrimental interface traps, is ascribed to mismatch induced dislocations, ESR thus pinpointing the nature of these atomic defects. (2) Annealing the c-Lu$_2$O$_3$/(111)Si entities at T$_{an}$ in the range as low as 420–550 °C in vacuum ($\leq 4 \times 10^{-6}$ Torr) already results in the formation of a SiO$_x$ IL, as evidenced by the observation of an increase in P$_b$ defect density and the appearance of the EX center, an SiO$_2$ associated defect. We should caution though that this apparent reduced thermodynamic stability as, e.g., compared to a-LaAlO$_3$/Si may result from the much higher oxygen diffusion coefficient in the Lu$_2$O$_3$ film system placed in a limited vacuum of insufficiently low partial O$_2$ pressure. The interface is observed to evolve to fully Si/SiO$_{2(x)}$-type at T$_{an} \sim 700$ °C, as signaled by the observed P$_b$ perfect density close to the natural density of (111)Si/SiO$_2$. For T$_{an} \geq 1000$ °C, the Si/SiO$_2$ nature of the IL starts to collapse, possible linked to disintegration of the Lu$_2$O$_3$ film altogether. (3) After standard H$_2$-passivation, a P$_b$ density of $\sim 5.8 \times 10^{11}$ cm^{-2} was observed, i.e., the standard H-passivation technique fails to deactivate the P$_b$'s (fast interface traps) to a (sub) 10^{10} cm^{-2} eV^{-1} level. This deficiency in passivation would limit the use of the crystalline Lu$_2$O$_3$ as a replacement for SiO$_2$ in future Si-based devices. (4) The inherent interface quality of the crystalline Lu$_2$O$_3$/(111)Si is superior to that of a-Lu$_2$O$_3$/(100)Si, where for the latter case, an Si/SiO$_2$-type interface of inferior quality is formed, present already after a PGA in vacuum at T$_{an} = 200$ °C, with no improvement for any higher T$_{an}$.

Within the interpretation concluding the observed P$_b$-type defects in epi-insulator/c-Si heterostructures with positive lattice mismatch (f) as inextricably bounded up with MDs, the latter would jeopardize the usefulness of c-(high-κ) dielectrics as gate insulators in general. To meet technological standards, these must be avoided, achievable by selecting systems with limited f and/or restricted dielectric epilayer thickness to below the relaxation limit set by mismatch stress. No conclusions are drawn for negative-f systems.

In addition to the ability to reveal atomic imperfections linked with hetero epitaxial growth on the very atomic scale, the ESR method appears adequate to monitor thermal (interface) evolution of layered structures.

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