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Fully transparent field-effect transistor with high drain current and on-off ratio Ⓕ

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ABSTRACT

We report a fully transparent thin-film transistor utilizing a La-doped $BaSnO_3$ channel layer that provides a drain current of 0.468 mA/μm and an on-off ratio of 1.5×10^8. The La-doped $BaSnO_3$ channel is grown on a 100–150 nm thick unintentionally doped $BaSnO_3$ buffer layer on a (001) MgO substrate by molecular-beam epitaxy. Unpatterned channel layers show mobilities of 127–184 cm^2 V^{-1} s^{-1} at carrier concentrations in the low to mid 10^{19} cm^{-3} range. The $BaSnO_3$ is patterned by reactive ion etching under conditions preserving the high mobility and conductivity. Using this patterning method, a sub-micron-scale thin film transistor exhibiting complete depletion at room temperature is achieved.

Transparent oxide thin-film transistors (TFTs) have been studied extensively for over a decade for applications that include displays, wearable electronics, and smart windows.[1–3] Due to the relatively high mobilities of the transparent oxide semiconductors used, when scaled to small dimensions, transparent oxide TFTs are expected to have high drain current (I_D, drain-to-source current per channel width) and low power consumption, which are important for energy-sensitive applications. Tin-based oxide systems are promising materials for transparent oxide TFTs due to the superior oxygen stability and high mobility of these materials at room temperature.[4,5] Among stannates, the transparent perovskite $BaSnO_3$ is attracting worldwide attention following the recent discovery that La-doped $BaSnO_3$ has both high mobility at room

temperature and excellent oxygen stability. Mobilities as high as 320 cm^2 V^{-1} s^{-1} and 183 cm^2 V^{-1} s^{-1} have been achieved in La-doped $BaSnO_3$ single crystals[4] and epitaxial thin films,[6] respectively, at room temperature. The high mobility of $BaSnO_3$ is attributed to the small effective mass originating from the large dispersion of the conduction band from the Sn 5s orbital,[7] high dielectric constant ($K \approx 20$)[8] which reduces dopant scattering,[4] and small phonon scattering.[9]

The performance of TFTs based on $BaSnO_3$ has been steadily improving in recent years, with the highest I_D achieved being 0.021 mA/μm.[10] This performance is limited by the large size of the $BaSnO_3$-based TFTs, which have channel dimensions of 100–200 μm. These large devices have been patterned using metal shadow

masks during growth, i.e., without photolithography. Attempts to use photolithography to define smaller devices have been plagued by the creation of oxygen vacancies in the BaSnO$_3$ film, including the undoped BaSnO$_3$ buffer layer, during the ion-milling process. These vacancies make the undoped BaSnO$_3$ buffer layer conductive, shunt the device, and degrade performance.[11] This problem is well known in other oxides as well.[12]

Here, we report growth of high mobility La-doped BaSnO$_3$ thin films on MgO substrates using molecular-beam epitaxy and use reactive ion etching (RIE) to pattern BaSnO$_3$–based TFTs. With appropriate conditions, this etching technique enables BaSnO$_3$ to be etched with a controllable etch rate while preserving surface roughness and electrical properties including conductivity and mobility. The resulting micrometer-scale photolithography defined BaSnO$_3$–based transparent TFT has a peak field-effect mobility of 17.2 cm^2/V^{-1} s^{-1}, an on-off ratio over 1.5×10^8, I_D over 0.468 mA/μm, and a peak transconductance (g_m) of 30.5 mS/mm. As we describe below, this is one of the highest performance fully transparent oxide TFTs ever reported.

Epitaxial La-doped BaSnO$_3$ films were grown on (001) MgO substrates by adsorption-controlled growth using molecular-beam epitaxy with barium, lanthanum, and SnO$_2$ sources. The details of the growth process are given elsewhere.[6] Epitaxial growth of single-phase La-doped BaSnO$_3$ on MgO substrates was confirmed by x-ray diffraction (XRD) measurements; the full width at half maximum of the BaSnO$_3$ 002 peak is 0.31° (see Fig. S1 of the supplementary material). MgO substrates, with a bandgap of about 7.8 eV,[13] are used to avoid the potential complications of persistent photoconductivity from the substrate arising from light exposure during the photolithography process.[14] On the MgO substrate, an undoped BaSnO$_3$ layer followed by a La-doped BaSnO$_3$ layer is grown to form the channel of the TFT as is typical for BaSnO$_3$-based TFTs.[10,15–19] The purpose of the undoped BaSnO$_3$ layer is to reduce the density of threading dislocations that propagate into the overlying doped (and conducting) BaSnO$_3$. Even with such a buffer layer, the threading dislocation density of BaSnO$_3$ films grown on MgO as well as other commonly used substrates is of order 10^{11} cm^{-2};[6,15,20] an ideal substrate for BaSnO$_3$ has yet to be demonstrated, but several lattice matched candidates are being developed.[21–23]

The heterostructures for TFTs fabrication consist of a 100–150 nm thick unintentionally doped BaSnO$_3$ buffer layer followed by about 10 nm of La-doped BaSnO$_3$. In test structures, the Hall mobility of a 10-nm-thick La-doped BaSnO$_3$ layer (grown on an MgO substrate with an undoped BaSnO$_3$ buffer layer) reaches 184 cm^2 V^{-1} s^{-1} at a carrier concentration of 6.5×10^{19} cm^{-3}. Despite the thin La-doped BaSnO$_3$ film and the use of a nonperovskite MgO substrate, this value is the highest mobility reported for BaSnO$_3$ thin films; it is slightly higher than the previous record achieved on a DyScO$_3$ substrate.[6] The Hall mobility of a 10-nm thick La-doped BaSnO$_3$ layer (on a 150 nm thick undoped BaSnO$_3$ buffer layer) with a carrier concentration of 1.3×10^{19} cm^{-3} is over 90 cm^2 V^{-1} s^{-1}. This decrease in mobility as the carrier concentration in La-doped BaSnO$_3$ is reduced below about 7×10^{19} cm^{-3} is typical of BaSnO$_3$ films[6,15,20] and is a result of scattering from the huge density of threading dislocations, which become less effectively screened from the mobile charge carriers as the carrier concentration is reduced.[4,20] The mobility, limited by the threading dislocations, is given by[24,25]

$$\mu_{td} = \frac{4ec^2}{Z^2\hbar N_{td}}\left(\frac{3n}{\pi^4}\right)^{2/3}(1+y(n))^{3/2},$$

where

$$y(n) = \frac{2\pi^2\hbar\varepsilon}{e^2 m^*}\left(3\pi^2 n\right)^{1/3}$$

and e, c, Z, N_{td}, n, ε, and m^* are the electron charge, c-axis lattice parameter, charge state of a unit cell in a threading dislocation, density of threading dislocations, carrier concentration, dielectric permittivity, and effective mass, respectively. The fitting parameters are given in the supplementary material. The fitting achieved using this formula is overall in good agreement with the experimental data (see Fig. S6 of the supplementary material). The mobilities of our La-doped BaSnO$_3$ films on MgO are the highest yet reported at the relatively low carrier concentrations and low thickness of La-doped BaSnO$_3$ layers,[4,15,26,27] which are needed to be able to fully deplete the TFT channel when a voltage is applied to the gate.

In order to make micrometer scale TFTs, it is critical to be able to lithographically pattern the high mobility La-doped BaSnO$_3$ channel layer without degrading its electrical performance. A few methods have been used in the past to pattern a La-doped BaSnO$_3$ channel layer. Early BaSnO$_3$ TFTs used shadow masks to define the channel structure during deposition.[10,15–19] This method can pattern the La-doped BaSnO$_3$ layer without degrading its surface roughness and electrical properties, but the channel length is limited to about 100 μm. More recently ion-milling has been employed to pattern the La-doped BaSnO$_3$ layer. Although ion-milling can etch La-doped BaSnO$_3$ to micrometer scale dimensions with controllable etch rate, the size of the channel length reported was about 100 μm.[11] Importantly, the resulting BaSnO$_3$ TFT with an undoped BaSnO$_3$ layer could not be depleted at room temperature and its on-off ratio was only 2. The reason for the inability to deplete the TFT at room temperature was attributed to significant charge trapping,[11] but our own experiments reveal that undoped BaSnO$_3$ becomes conductive when subjected to ion-milling. The conductivity of an undoped BaSnO$_3$ layer increased more than 10^8 times following ion-milling even when we use the smallest available acceleration voltage of our equipment, 400 V. Such an enhancement in conductivity of the undoped BaSnO$_3$ layer is consistent with it is being caused by the creation of oxygen vacancies from the high energy bombardment of Ar ions during the ion-milling process, as has been reported for SrTiO$_3$.[12]

The undesired conductance enhancement in unintentionally doped BaSnO$_3$ resulting from ion-milling can be reduced by annealing the sample in flowing oxygen at temperatures of about 800 °C, but even after such aggressive annealing, the conductance does not fully return to its original state. The effect of annealing on ion-milled undoped BaSnO$_3$ in flowing O$_2$ at temperatures from 300 °C to 800 °C is given in the supplementary material (see Fig. S7 of the supplementary material). Therefore, we believe that the conductance of the underlying undoped BaSnO$_3$ buffer layer caused by the ion-milling process is partially responsible for the poor room-temperature performance of the prior BaSnO$_3$-based TFT device subjected to ion-milling.[11] Ion-milling can also alter film stoichiometry and lead to charge trapping from defects along the side walls. For this reason, we have developed an alternate etching process to pattern the BaSnO$_3$ layers into a TFT.

In order to overcome the limitations of previous techniques used to define BaSnO$_3$-based TFTs, we employ reactive-ion etching (RIE) using chlorine and argon gases to etch the BaSnO$_3$ epitaxial stack. By using a reactive gas such as chlorine, the RIE technique can etch a BaSnO$_3$ film with a chemical process rather than a purely physical process, in contrast to ion-milling. Under appropriate conditions, the undoped BaSnO$_3$ film conductivity issue that we ascribe to the creation of oxygen vacancies can be resolved. Furthermore, with RIE, we are able to achieve a controllable etch rate that is not dependent on sample quality. In short, our RIE etching process for BaSnO$_3$ provides a controllable etch rate while preserving surface roughness and electrical properties including conductivity and mobility—qualities critical to the fabrication of high-performance TFTs. BCl$_3$ gas can also be used for RIE etching of BaSnO$_3$ while preserving surface roughness and electrical properties including conductivity and mobility, but the etch rate is lower than when chlorine gas is used. Therefore, using chlorine gas without adding BCl$_3$ gas is preferable. A higher etch rate is desirable to reduce etch time, but there is a trade-off between the etch rate and damage to the BaSnO$_3$ film. In making the TFTs, the etch rate has been maximized without damaging the properties of the BaSnO$_3$ film by adjusting RIE etching parameters. The RF power of the RIE is around 80–120 W with a DC voltage in the 200–250 V range. The total gas pressure is around 1–2 mTorr, and a gas ratio between 1:5 and 5:1 is used for the Cl$_2$ and Ar gases.[28]

The device patterning and fabrication process was completed in the cleanroom environment of Cornell's NanoScale Science and Technology Facility (CNF), except for the atomic layer deposition (ALD) process. For light exposure during photolithography, an Autostep 200 stepper was used. The channel layer was etched using a PT720/740 RIE etching tool. For device isolation, the channel layer was etched down about 18 nm, considerably beyond the 10 nm thickness of the La-doped BaSnO$_3$ top layer and well into the undoped BaSnO$_3$ buffer layer. After the etching process, indium tin oxide (ITO) was deposited as source and drain contacts using a PVD75 sputtering tool. The source and drain contacts were patterned by lift-off. A blanket HfO$_2$ gate dielectric layer was then deposited over the full structure by atomic-layer deposition (ALD), at 300 °C with ozone as an oxidant, which leads to have a deposition rate of 0.8 Å/cycle. The thickness of the HfO$_2$ layer was 20 nm. To complete the TFT, ITO was deposited again on the gate dielectric to form the gate electrode using the same sputtering tool as used earlier in the process. The gate contact was also patterned by lift-off. Electrical measurements were performed using a Cascade probe station with a Keithley 4200 SCS system. All device measurements presented were measured at room temperature in ambient air.

Figure 1 shows a schematic of the BaSnO$_3$–based TFT measured in Figs. 2 and 3, together with a scanning electron microscope image of the fully patterned device. The mobility and carrier concentration of the as-grown La-doped BaSnO$_3$ channel layer in this sample are μ = 65.2 cm^2 V^{-1} s^{-1} and n = 1.81 × 10^{19} cm^{-3}, respectively, from Hall measurements at room temperature. The channel length and width of the TFT are L = 0.3 μm and W = 0.93 μm, respectively. This is the smallest BaSnO$_3$–based TFT yet reported.[10,11,15–19] Further scaling is limited by the resolution of the light exposing tool.

The characteristic curves of the BaSnO$_3$ TFT are shown in Fig. 2. Figure 2(a) shows the transfer characteristic of the device: I_D vs V_{GS} (gate-to-source voltage) and μ_{FE} (field-effect mobility)
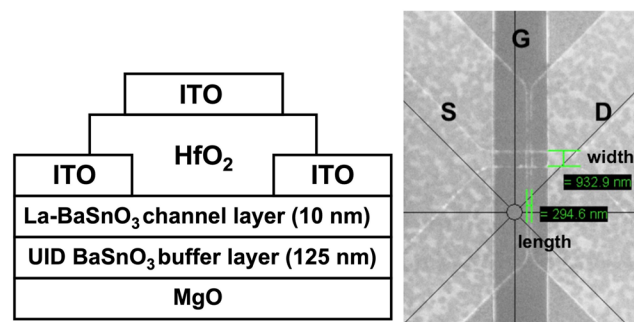

FIG. 1. Schematic and scanning electron microscope image of the BaSnO$_3$ TFT device. The channel is 0.3 μm long and 0.93 μm wide.

vs V_{GS}. As shown in Fig. 2(a), the TFT can be depleted completely at room temperature—a first for a photolithographically defined BaSnO$_3$-based TFT.[11] The field-effect mobility of the device is calculated from the relation $\mu_{FE} = \left(\frac{L}{C_{ox} W V_{DS}} \right) \frac{\partial I_{DS}}{\partial V_{GS}}$.[30] I_{DS}, L, C_{ox}, and W are the drain-to-source current, the channel length, the capacitance of the gate dielectric per unit area, and the channel width, respectively. The capacitance of the HfO$_2$ gate dielectric was measured as shown in Fig. S9 of the supplementary material with a metal-oxide semiconductor (MOS) structure with dimensions 50 μm × 50 μm. This MOS capacitor has the same La-doped BaSnO$_3$ channel layer and the same ITO gate electrode as the TFT, i.e., the layers measured in the MOS capacitor were deposited on the MgO wafer and patterned into the MOS capacitor test structure and into the TFT. For calculating μ_{FE}, the maximum C_{ox} at the given voltage range has been used so as to not overestimate μ_{FE}. The calculated μ_{FE} is 17.2 cm^2 V^{-1} s^{-1}. The large difference between the field-effect mobility and the Hall mobility can be attributed to the contact resistance. The contact resistance includes the sheet resistance of the ITO contact layer and interface resistance between the ITO contact layer and the La-doped BaSnO$_3$ channel layer. In the supplementary material (see Fig. S10), we utilize the measured value of the contact resistance to calculate the field-effect mobility; the result is 72 cm^2 V^{-1} s^{-1}, which is comparable to the Hall mobility of the as-grown channel layer. From the details of this calculation, it is clear that the high contact resistance is significantly limiting the TFT performance; a lower resistance contact will increase the field-effect mobility and thus the drain current. There is dispersion in the capacitance at measurement frequencies higher than 100 kHz, and it is believed to be related to the trapping of charge by defects or impurities within the HfO$_2$ film and at the interface between the HfO$_2$ and La-doped BaSnO$_3$ channel layer since the cutoff frequency is 51.6 MHz. The cutoff frequency is calculated from the relation $f = \frac{1}{2\pi RC}$ and is much higher than 100 kHz. The on-off ratio is over 1.5 × 10^8. This is the highest on-off ratio among BaSnO$_3$ TFTs when an undoped BaSnO$_3$ buffer layer is used.[10,11,15–18] The subthreshold swing has been calculated from the equation $S = \left(\frac{\partial \log I_{DS}}{\partial V_{GS}} \right)^{-1}$, and S is 0.15 V dec^{-1}. Figure 2(b) shows the transconductance of the device at V_{DS} = 1 V as a function of V_{GS}. The transconductance is calculated from the relation $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$. The maximum transconductance is 30.5 mS/mm
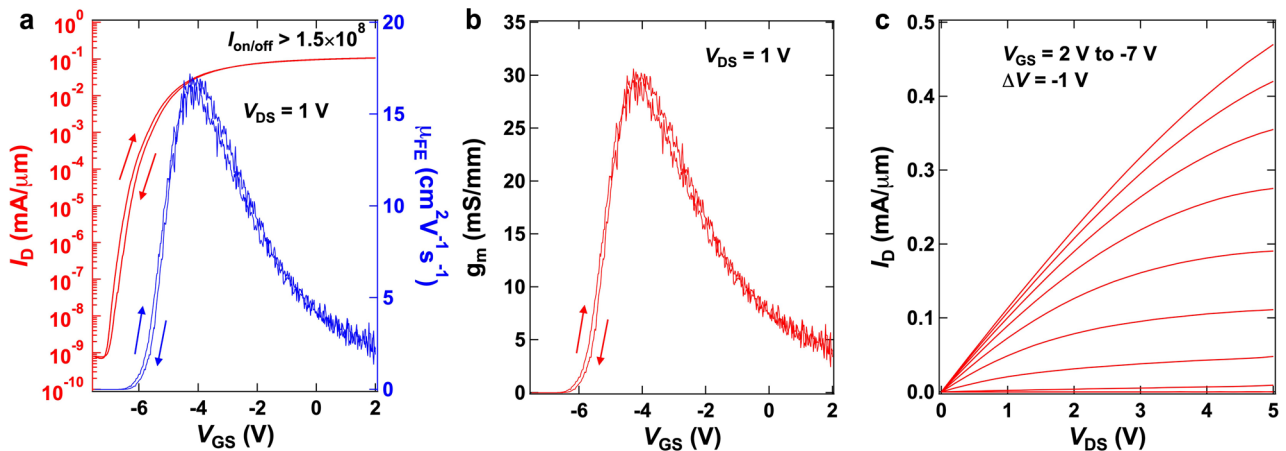
FIG. 2. (a) The transfer characteristic of the TFT based on La-doped BaSnO$_3$ at V_{DS} = 1 V and the field-effect mobility. The peak field-effect mobility is 17.2 cm^2 V^{-1} s^{-1}, and the on-off ratio is over 1.5 × 10^8. The subthreshold swing is 0.15 V dec^{-1}. (b) Transconductance of the device at V_{DS} = 1 V. The maximum transconductance is 30.5 mS/mm. (c) The output characteristic of the device at V_{GS} = 2, 1, 0, −1, −2, −3, −4, −5, −6, −7 V. The maximum drain current exceeds 0.467 mA/μm.

at V_{DS} = 1 V. This is much higher than the previous record transconductance in a BaSnO$_3$ based TFT, which is only 2 mS/mm.[11] Figure 2(c) shows the output characteristic of the device, which is I_D vs V_{DS} (drain-to-source voltage) by varying V_{GS} from 2 to −7 V. As shown in Fig. 2(c), the drain current reaches over 0.468 mA/μm. The slow increase in the drain current with respect to V_{DS} is attributed to the high contact resistance. The resistance of the ITO/La-doped BaSnO$_3$/ITO channel structure vs channel length is plotted in Fig. S10 of the supplementary material. The source/drain contact resistance between the ITO contact layer and the La-doped BaSnO$_3$ channel layer, which is 5.1 kΩ μm, is calculated by
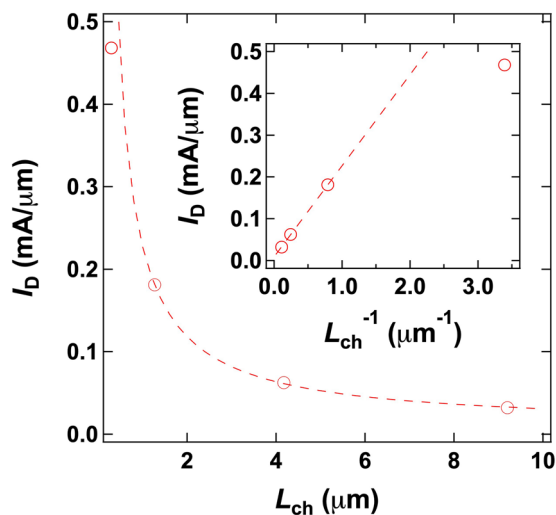

FIG. 3. Drain current dependence on channel length (L_{ch}) when V_{GS} = 2 V and V_{DS} = 5 V. The drain current (I_D) is inversely proportional to the overall channel length except at the shortest channel length, showing little degradation with respect to device scaling. The deviation from linear behavior in the inset at the shortest channel length is likely due to the contact resistance and not short channel effects such as velocity saturation.

extrapolating a linear fit to the plot. The high contact resistance affects the slow response of I_D vs V_{DS} in the measured output characteristics as shown in Fig. S11 of the supplementary material; thus, the drain current can be improved by lowering the contact resistance.

The drain current vs channel length at V_{GS} = 2 V and V_{DS} = 5 V is plotted in Fig. 3. The drain current is inversely proportional to the overall length of the channel except at the shortest channel length of 0.3 μm, showing little degradation with respect to device scaling. The close agreement between the calculated field-effect mobility (with the effect of contact resistance included) and Hall mobility indicates that the deviation from linear behavior at the short channel length of 0.3 μm in the inset of Fig. 3 is likely due to the contact resistance and not short channel effects such as velocity saturation. At a channel length of 0.3 μm, the channel resistance is comparable to the contact resistance and the effective voltage applied to the channel is greatly diminished, lowering drain current. A lower resistance contact is expected to reduce the deviation evident in Fig. S11 (a) between the ideal square-law transistor model and actual TFT performance.

The interface trap charge density D_{it} can be calculated using[31]

$$S = \frac{kT \ln 10}{e}\left(1 + \frac{e^2}{C_{ox}}D_{it}\right),$$

where k, T, and e are the Boltzmann constant, temperature, and electron charge, respectively. The calculated D_{it} is 5.03×10^{12} eV^{-1} cm^{-2}.

A comparison of the drain current vs on-off ratio among transparent oxide channel TFTs is shown in Fig. 4.[3,5,10,15–19,32–57] The high I_D of the highest performance TFT with a transparent oxide channel was achieved on cleaved and transferred flakes of β-Ga$_2$O$_3$ onto an opaque substrate;[48] this is not a scalable technology. These data are indicated as gray marks. Our BaSnO$_3$-based TFT exhibits one of the best performances of all transparent oxide TFTs and is comparable to the best TFTs made with transparent oxide channel materials (in device structures in which other elements are not transparent). Its drain current is second best among all fully transparent scalable oxide channel TFTs.[57]
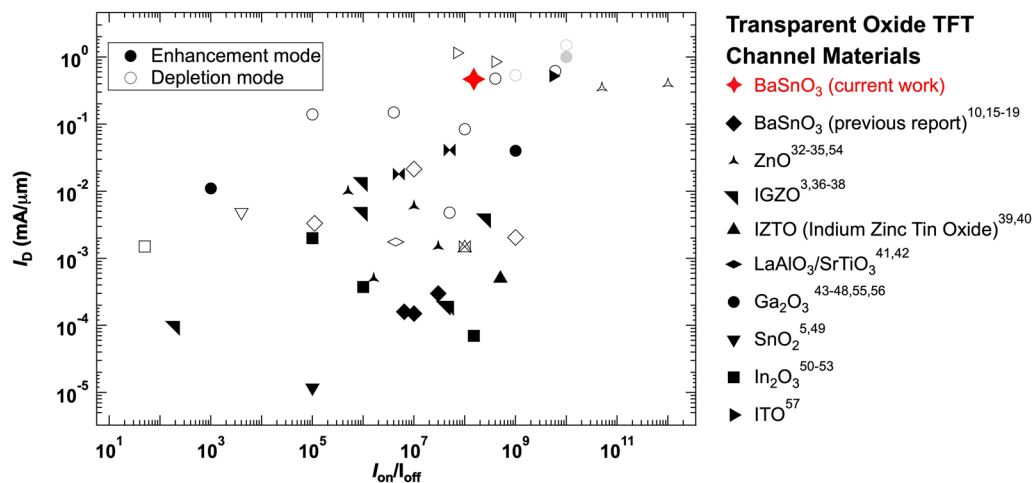
FIG. 4. Comparison of drain current in TFTs with transparent oxide channels with respect to the on/off current ratio. The drain current of the BaSnO₃ TFT described in this article is the highest value among all transparent oxide channel field-effect transistors. The solid symbols represent enhancement-mode TFT devices, and the hollow symbols represent depletion-mode TFT devices. The top right corner is the desired corner of the plot for the best TFT performance.

In summary, a fully transparent submicron TFT based on $BaSnO_3$ has been fabricated with a high drain current and on/off current ratio. This breakthrough is made possible by (1) high mobility bare films in combination with (2) the development of a micrometer-scale etching method that preserves the surface roughness, conductivity, and mobility of $BaSnO_3$ films. These results demonstrate the tremendous potential of $BaSnO_3$ for the future of transparent electronics.

SUPPLEMENTARY MATERIAL

See the supplementary material for further data and discussion of the structural and electrical properties. This includes X-ray diffraction θ-2θ and ϕ-scans, a reflection high-energy electron diffraction (RHEED) intensity oscillation during the growth of a $BaSnO_3$ thin film, a reciprocal space map (RSM) of a $BaSnO_3$ thin film, atomic force microscope (AFM) images of the surface of a La-$BaSnO_3$ film before and after etching in dilute nitric acid, a plot of mobility vs carrier concentration for the La-$BaSnO_3$/undoped $BaSnO_3$/MgO heterostructures, a comparison of the 2-probe resistance of RIE-etched $BaSnO_3$ and ion-milled $BaSnO_3$ films following post annealing in flowing O_2, the band diagram of the $BaSnO_3$-based TFT device fabricated with a HfO_2 gate dielectric and an ITO gate contact, the capacitance vs V_{GS} characteristics of an MOS ITO/ALD-grown HfO_2/La-$BaSnO_3$ capacitor, extraction of the contact resistance from the ITO/La-doped $BaSnO_3$/ITO channel structure, analysis of the field-effect mobility that includes the high contact resistance, and a simulation of the ideal output characteristics of the $BaSnO_3$-based FET.

ACKNOWLEDGMENTS

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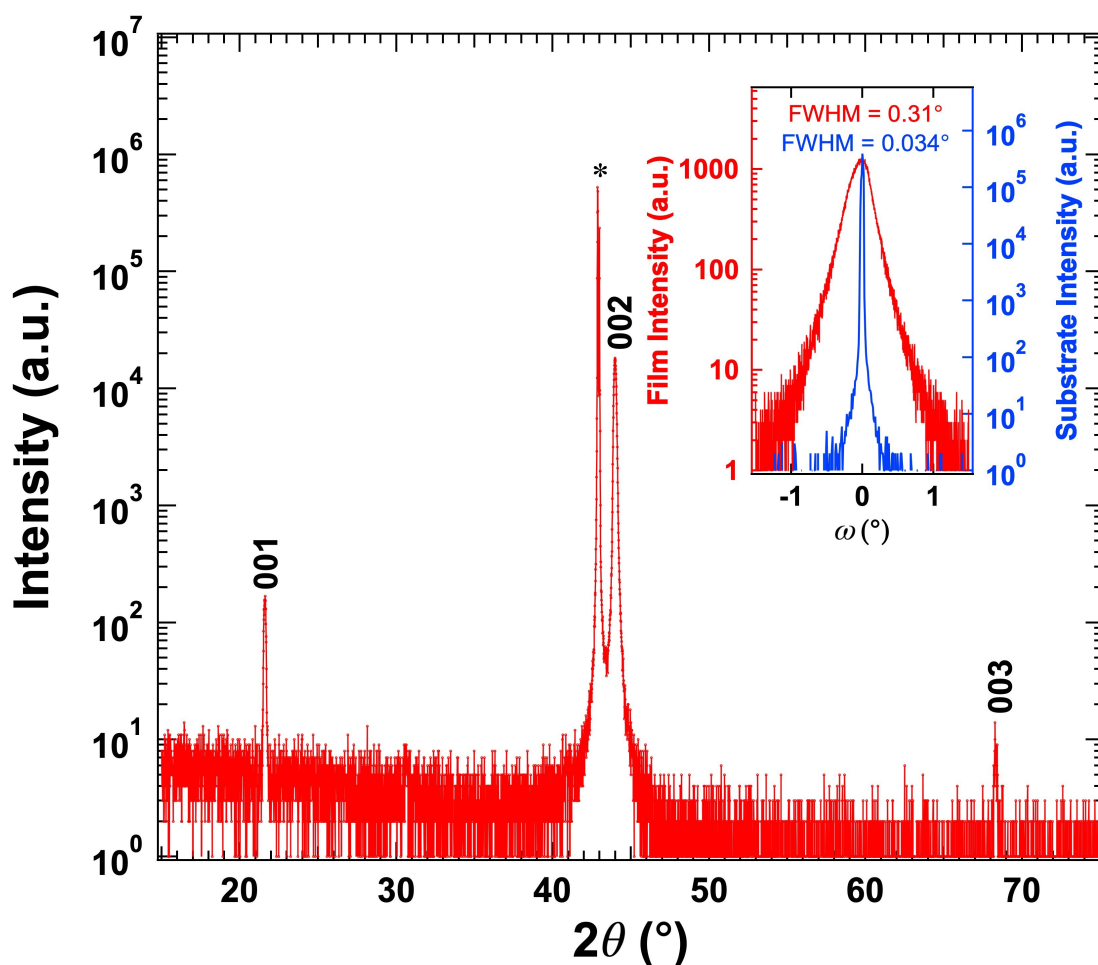
Supplementary Fig. S1. X-ray diffraction scan of a 10 nm thick La-BaSnO$_3$ thin film grown on a 120 nm thick undoped BaSnO$_3$ buffer layer on a (001) MgO substrate. The θ-2θ scan in combination with RHEED images confirms that the BaSnO$_3$ film grows epitaxially on the MgO substrate without any secondary phases. The inset shows the 002 BaSnO$_3$ rocking curve with a full width at half maximum (FWHM) of 0.31° and the 002 MgO rocking curve with a FWHM of 0.034°. This is the smallest value achieved for a BaSnO$_3$ film grown on an MgO substrate (Ref. S1)
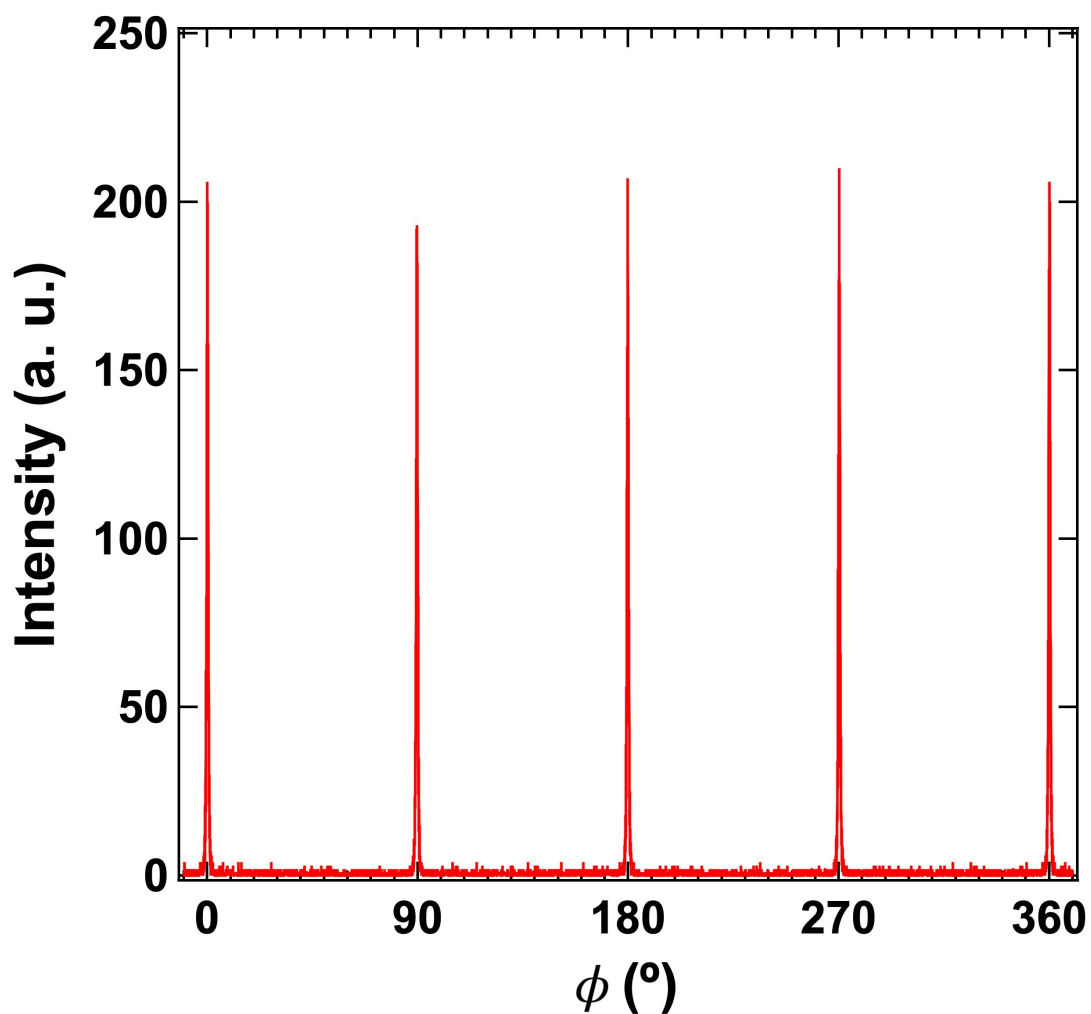
Supplementary Fig. S2. X-ray diffraction ϕ-scan of the 101 BaSnO₃ peaks of a 10 nm thick La-doped BaSnO₃ thin film grown on a (001) MgO substrate with a 120 nm thick undoped BaSnO₃ buffer layer. The ϕ-scan confirms that the BaSnO₃ film grows epitaxially on the MgO substrate.
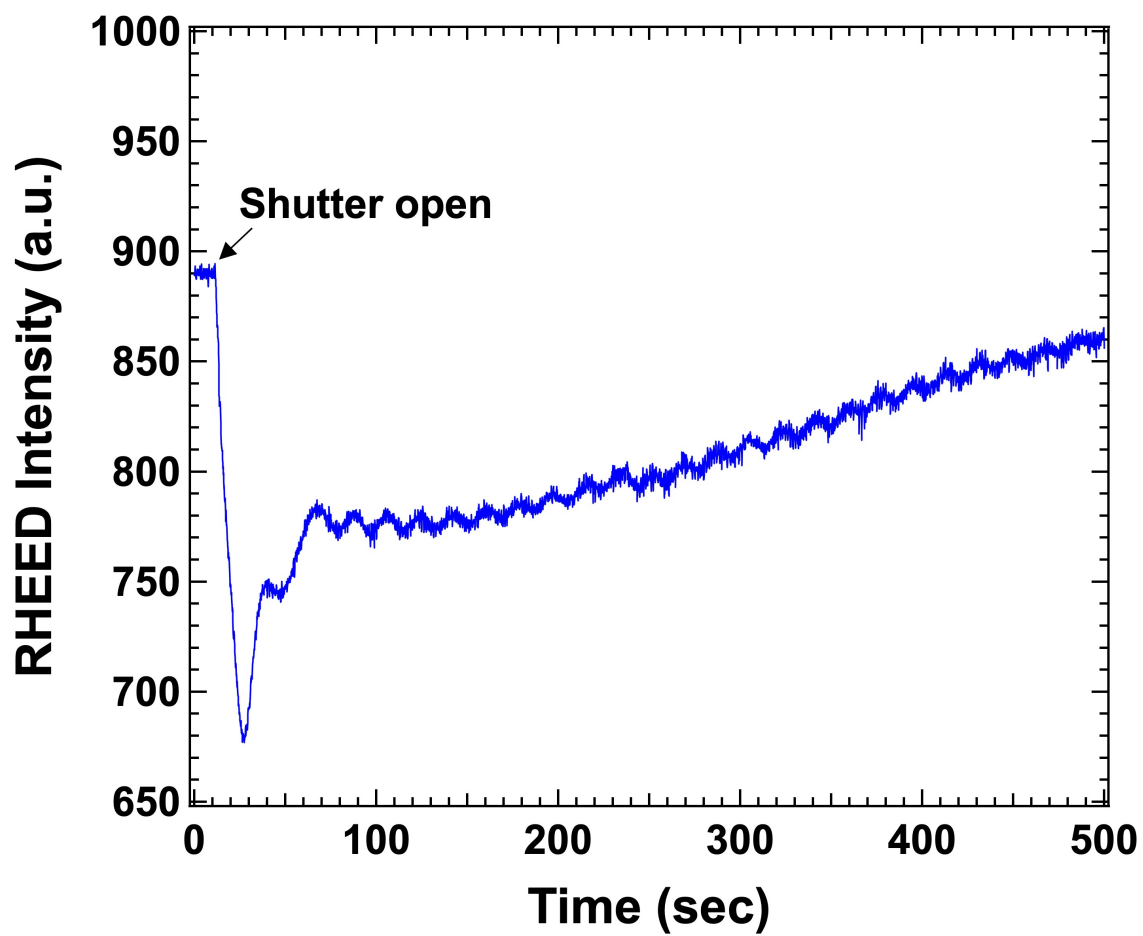
Supplementary Fig. S3. Reflection high-energy electron diffraction (RHEED) intensity oscillation during the growth of an undoped BaSnO$_3$ buffer layer on a (001) MgO substrate.
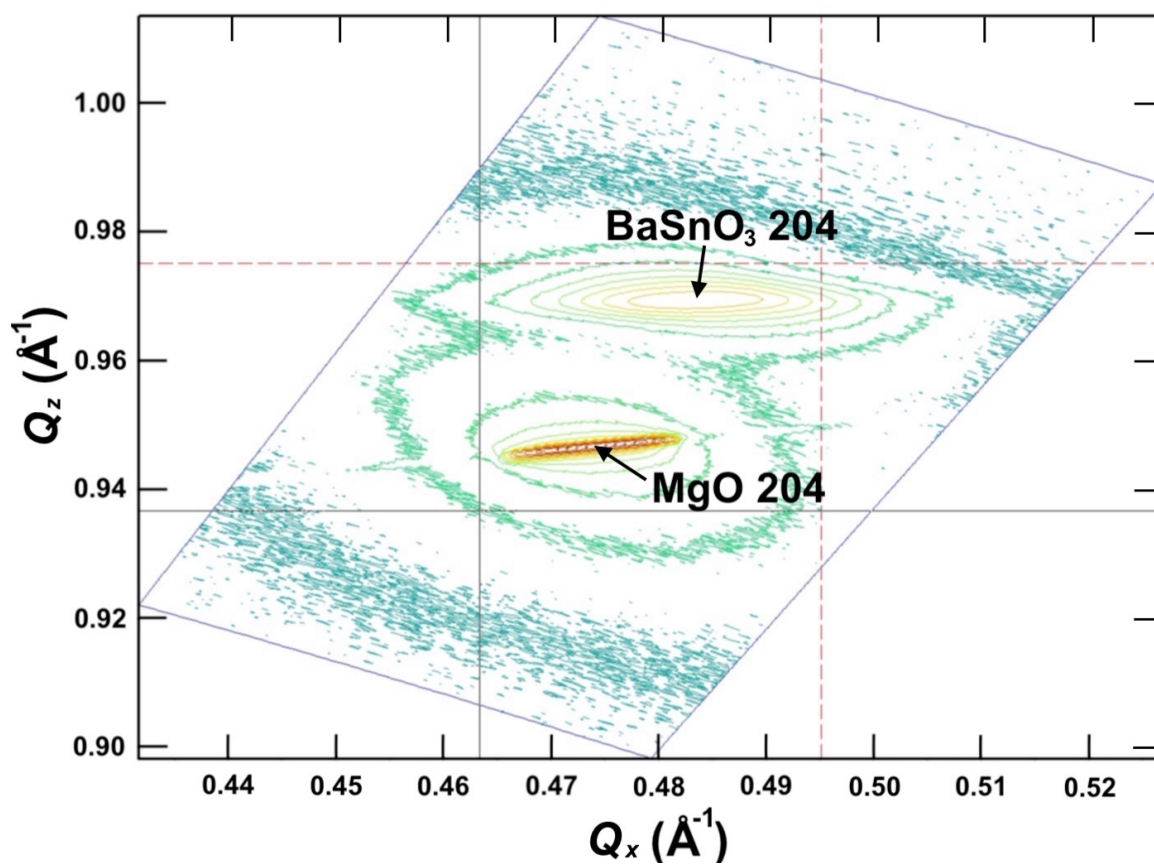
Supplementary Fig. S4. Reciprocal space map of a BaSnO$_3$ thin film grown on a (001) MgO substrate. The in-plane lattice parameter of the BaSnO$_3$ film is 4.127 Å and the out-of-plane lattice parameter is 4.113 Å. The FWHM of the 204 BaSnO$_3$ reflection at $\omega = 30.36°$ and $2\theta = 113.66°$ is 0.28° in ω.
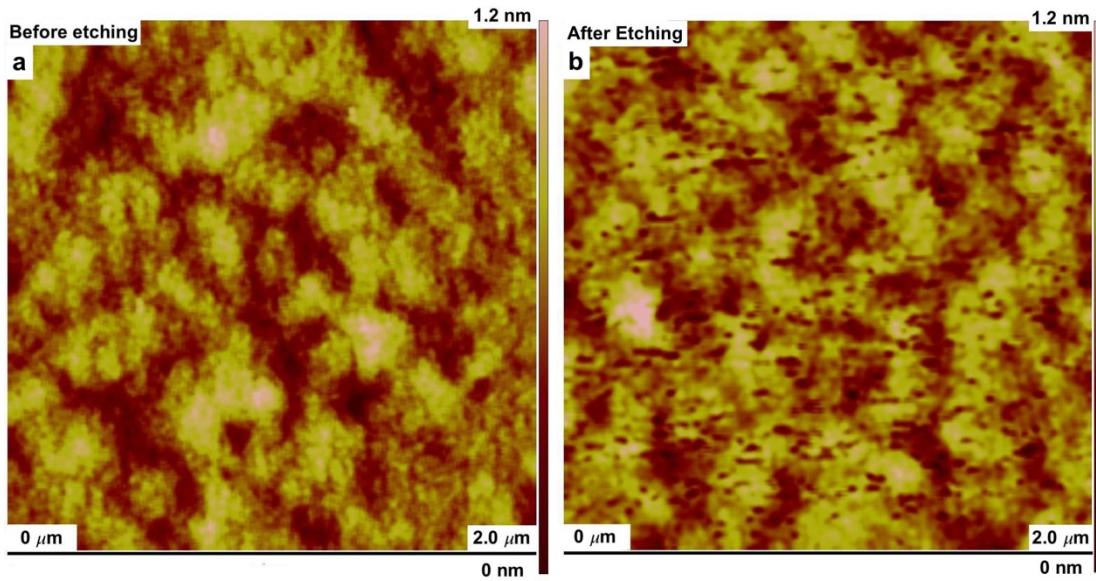
Supplementary Fig. S5. Atomic force microscope images of the surface of a 10 nm thick La-BaSnO$_3$ film with a 150 nm thick undoped BaSnO$_3$ buffer layer **(**a) before and (b) after etching in dilute nitric acid, revealing etch pits corresponding to a threading dislocation density of 8.0×10^{10} cm^{-2}.

The 10 nm thick La-BaSnO$_3$ film with a 150 nm thick undoped BaSnO$_3$ buffer layer grown on (001) MgO was etched in 0.5 % nitric acid for 10 s and the surface was scanned by an atomic force microscope (AFM). The AFM image shows a threading dislocation density of 8.0×10^{10} cm^{-2} in the sample.
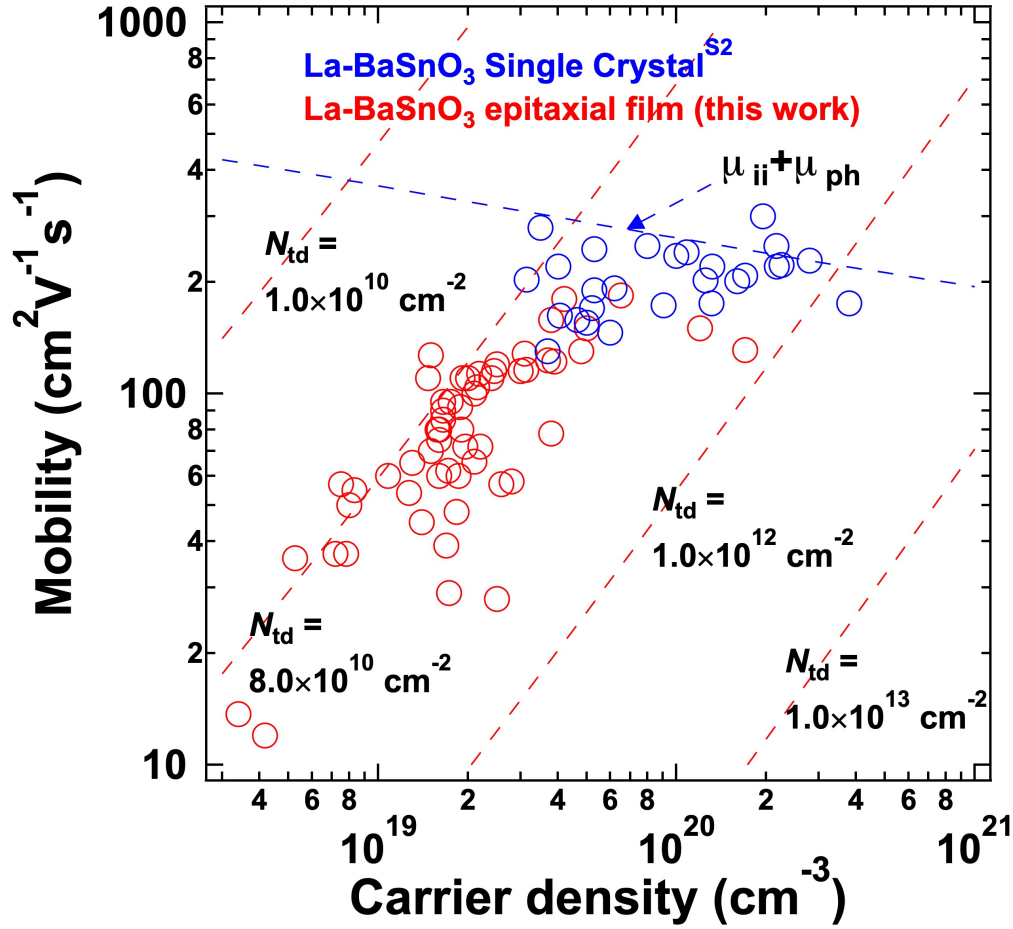
Supplementary Fig. S6. The mobility vs. carrier concentration of the La-BaSnO$_3$/undoped BaSnO$_3$/MgO heterostructures with that of single crystal La-BaSnO$_3$ for comparison (Ref. S2) The thicknesses of the La-BaSnO$_3$ and undoped BaSnO$_3$ layers are around 10 nm and 100-150 nm, respectively. A data of mobility of 181 cm^{2}V^{-1}s^{-1} at carrier concentration of 4.2×10^{19} cm^{-3} with 25 nm thick La-BaSnO$_3$ and 136 nm thick BaSnO$_3$ has been included in this plot. A record high mobility of 184 cm^{2}V^{-1}s^{-1} in BaSnO$_3$ thin films has been achieved even with the thin La-doped BaSnO$_3$ (10 nm) and undoped BaSnO$_3$ buffer layer. The dashed red lines are from the formula of the threading dislocation limited mobility for different threading dislocation densities (N_{td}) and $Z = 5.2$. The measured mobilities fit well with expectations from this formula at the given low carrier concentrations using a threading dislocation density of 8.0×10^{10} cm^{-2}.

The mobility limited by threading dislocation density is calculated from: [S3,S4]

$$\mu_{td} = \frac{4ec^2}{Z^2 \hbar N_{td}} \left(\frac{3n}{\pi^4}\right)^{\frac{2}{3}} \left(1 + y(n)\right)^{\frac{3}{2}},$$

where

$$y(n) = \frac{2\pi^2 \hbar \varepsilon}{e^2 m^*} (3\pi^2 n)^{1/3}.$$

The values of c = 4.113 Å and N_{td} = 8.0×10^{10} cm^{-2} are experimentally measured. The values of ε and m^*, 20 ε_0 and 0.42 m_0, where ε_0 and m_0 are the dielectric permittivity of vacuum and the rest mass of an electron, respectively, are taken from the literatures.[S5,S6] Z is calculated to be 5.2 by fitting the curve at N_{td} of 8.0×10^{10}. All of the dashed red lines in supplementary Fig. 6 indicating the variation of μ_{td} with threading dislocation density are calculated using the same Z value. The dashed lines showing the expected dependence of the mobility are overall in reasonable agreement with the experimental mobility measured on many samples possessing a range of carrier densities.

The mobility of single crystalline La-BaSnO$_3$ is presented for comparison. The mobility behavior fits well with the mobility calculated from the combination of ionized impurity scattering and phonon scattering as shown in Ref. S7. The ionized impurity scattering limited mobility and phonon scattering limited mobility are given by:[S3]

$$\mu_{ii} = \frac{24\pi^3\varepsilon^2\hbar^3 n}{Z^2 q^3 m^{*2} N_{ii}}\left[ln(1 + y(n)^2) + \frac{y(n)}{1 + y(n)}\right]^{-1}$$

and

$$\frac{1}{\mu_{300K}} = \frac{1}{\mu_{2K}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu(T)}.$$

Z and N_{ii} are the charge state of the ionized impurity and density of the ionized impurities, respectively. The phonon limited mobility is calculated to be 661 cm^{2}V^{-1}s^{-1}.[S7] The mobility of single crystalline La-BaSnO$_3$ is given by

$$\frac{1}{\mu_{SC,La-BaSnO_3}} = \frac{1}{\mu_{ii}} + \frac{1}{\mu_{ph}}.$$
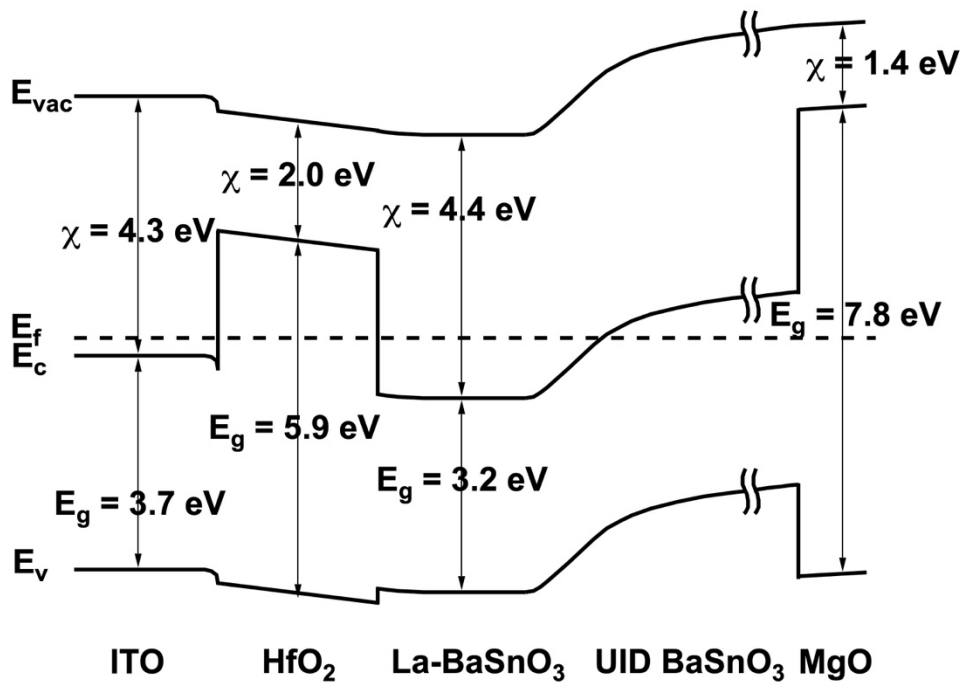
From this relation, the mobility of single crystalline La-BaSnO$_3$ that includes the effects of ionized impurity scattering and phonon scattering is obtained.
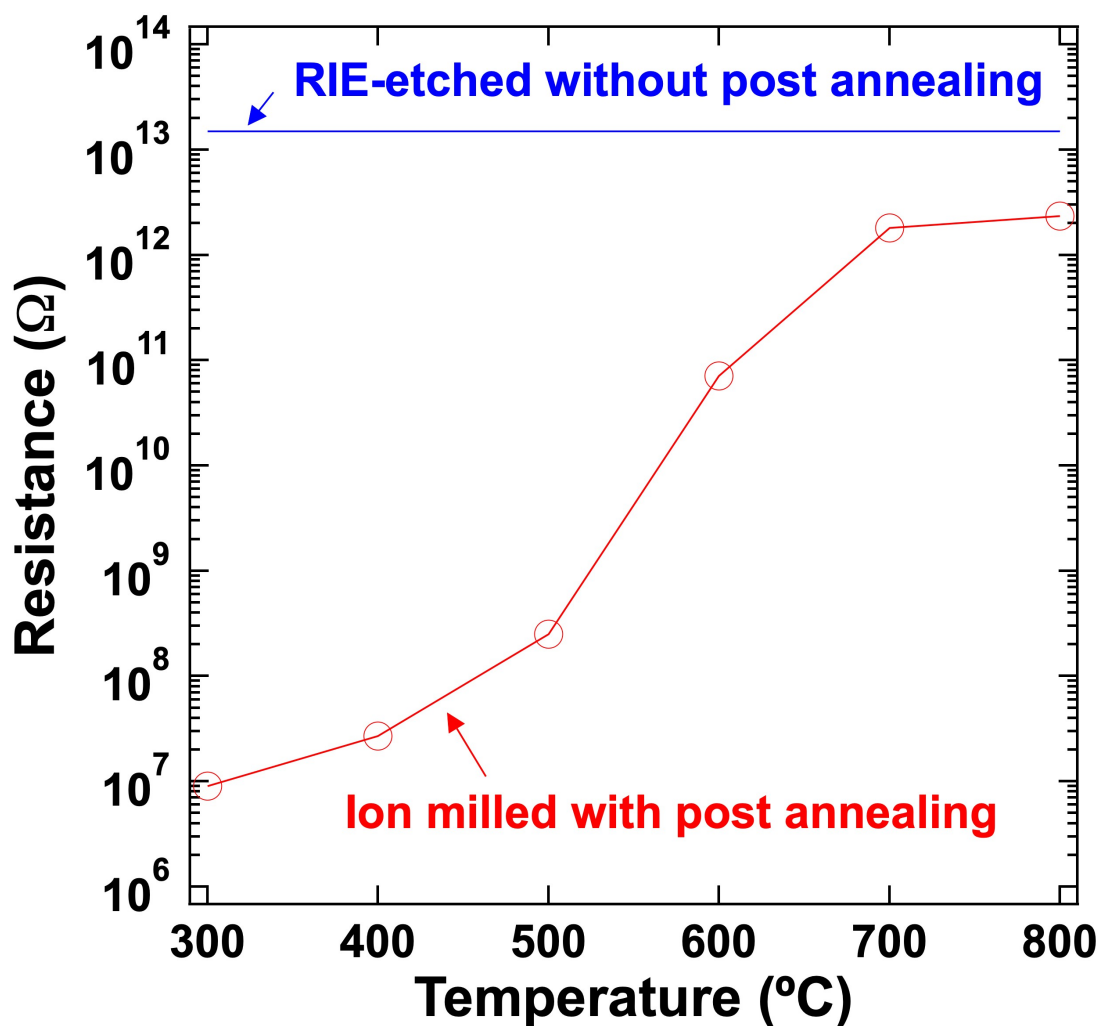
Supplementary Fig. S7. Comparison of 2-probe resistance at the surfaces of RIE-etched $BaSnO_3$ and ion-milled $BaSnO_3$ with post annealing in O_2 flow.

We annealed an ion-milled undoped $BaSnO_3$ sample in flowing O_2 at temperatures from 300 °C to 800 °C. At each temperature the sample was annealed for 2 hours. The resistivity of the sample was measured by a 2-probe measurement after each anneal. The result is plotted below. As can be seen from the plot, the resistivity of the undoped $BaSnO_3$ cannot be recovered by annealing at any temperature in the 300 °C to 600 °C range. Annealing at 700 °C and 800 °C improves the film resistivity, but it is still lower than that of the as-grown $BaSnO_3$ film and RIE-etched $BaSnO_3$. The resistivity of RIE-etched $BaSnO_3$ and that of undoped $BaSnO_3$ are the same (within the precision of our 2-point resistance

measurement). Also, using ion milling followed by a high-temperature annealing step above 700 °C is not desired due to possible damage to the sidewall by the ion-milling process and the loss of volatile constituents (SnO_x) from the $BaSnO_3$ during the high-temperature anneal.

$\chi = 1.4$ eV

$\chi = 2.0$ eV

$\chi = 4.3$ eV

$\chi = 4.4$ eV

E_{vac}

E_f
E_c

$E_g = 7.8$ eV

$E_g = 5.9$ eV

$E_g = 3.2$ eV

$E_g = 3.7$ eV

E_v

ITO   HfO$_2$ La-BaSnO$_3$ UID BaSnO$_3$ MgO

Supplementary Fig. S8. Band diagram of a BaSnO$_3$-based TFT device with a HfO$_2$ gate dielectric and an ITO gate contact with relevant data from Refs. S8-S14. The trapping of charges occurs at the interface between HfO$_2$ and BaSnO$_3$ due to defects and impurities in the HfO$_2$ film.
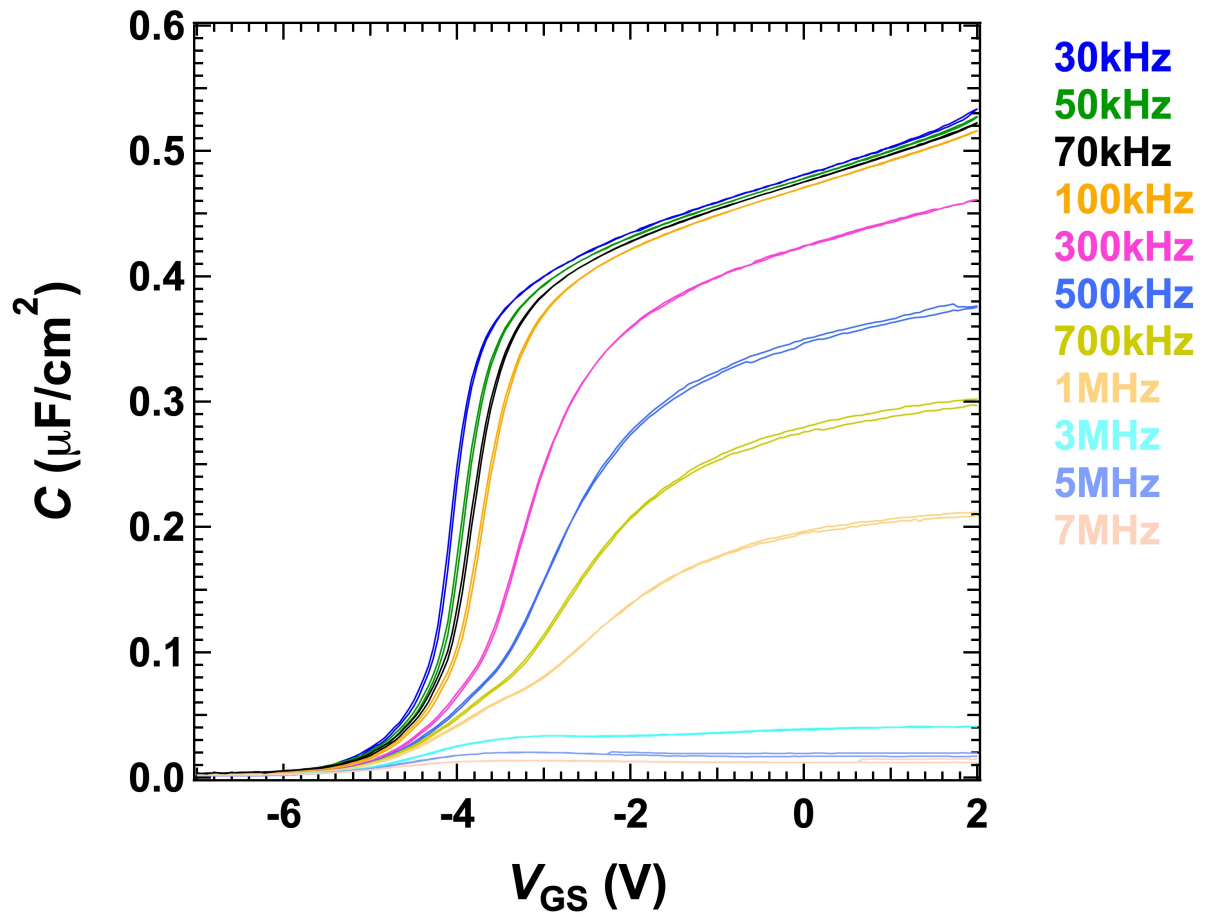
Supplementary Fig. S9. Capacitance (C_p) vs. V_{GS} characteristics of an MOS ITO/ALD-grown HfO_2/La-BaSnO$_3$ capacitor made with the same deposition conditions as the gate dielectric used for the BaSnO$_3$-based TFTs studied.
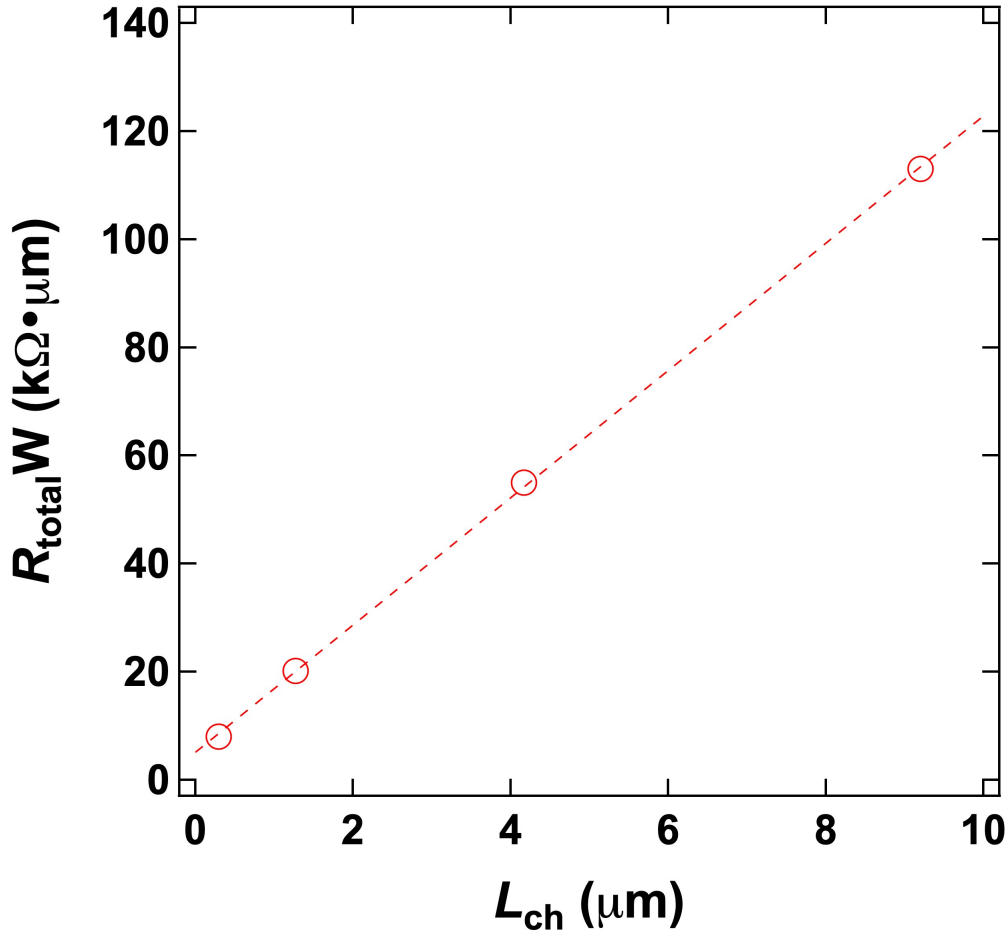
Supplementary Fig. S10. Extraction of contact resistance of an ITO/BaSnO$_3$/ITO channel structure with respect to the distance between the contacts. The contact resistance is estimated by extrapolating a linear fit to the data of total channel resistance (R_{total}W) vs. channel length (L_{ch}). The estimated contact resistance of the ITO layer is 5.1 k$\Omega\cdot\mu$m. The high contact resistance of the ITO source-drain contacts slows down the increase of the drain current as V_{GS} increases.

Our calculation of the field-effect mobility is 72 cm^{2}V^{-1}s^{-1}, which is comparable to the

Hall mobility of the as-grown channel layer. The details of this calculations are as follows.

From Supplementary Fig. S10, the contact resistance of ITO is 0.51 $\Omega\cdot$cm. The normalized

resistance of the La-BaSnO$_3$ channel with respect to the channel width is calculated by $R_s \times L$,

where R_s and L are sheet resistance and channel length, respectively. A sheet resistance of

5.4 kΩ/sq was measured by a Hall measurement and the channel length is 0.3 μm, giving a

channel resistance of 0.16 $\Omega\cdot$cm. When we apply V_{DS} = 1 V, the actual voltage applied to the

channel is given by $V_{channel} = \frac{R_{channel}}{R_{ITO}+R_{channel}} V_{DS} = 0.24$ V. This is only a fraction of V_{DS} due

to the high contact resistance of the ITO. Replacing V_{DS} by $V_{channel}$ in the equation $\mu_{FE} = \left(\frac{L}{C_{ox}WV_{DS}}\right)\frac{\partial I_{DS}}{\partial V_{GS}}$ yields the field-effect mobility, 72 cm^{2}V^{-1}s^{-1}. This is comparable to the mobility of the as-grown channel layer (65.2 cm^{2}V^{-1}s^{-1}), which was determined by the Hall effect. From the details of this calculation is it clear that a lower resistance contact would make $V_{channel}$ closer to V_{DS} and increase the field-effect mobility and thus the drain current.
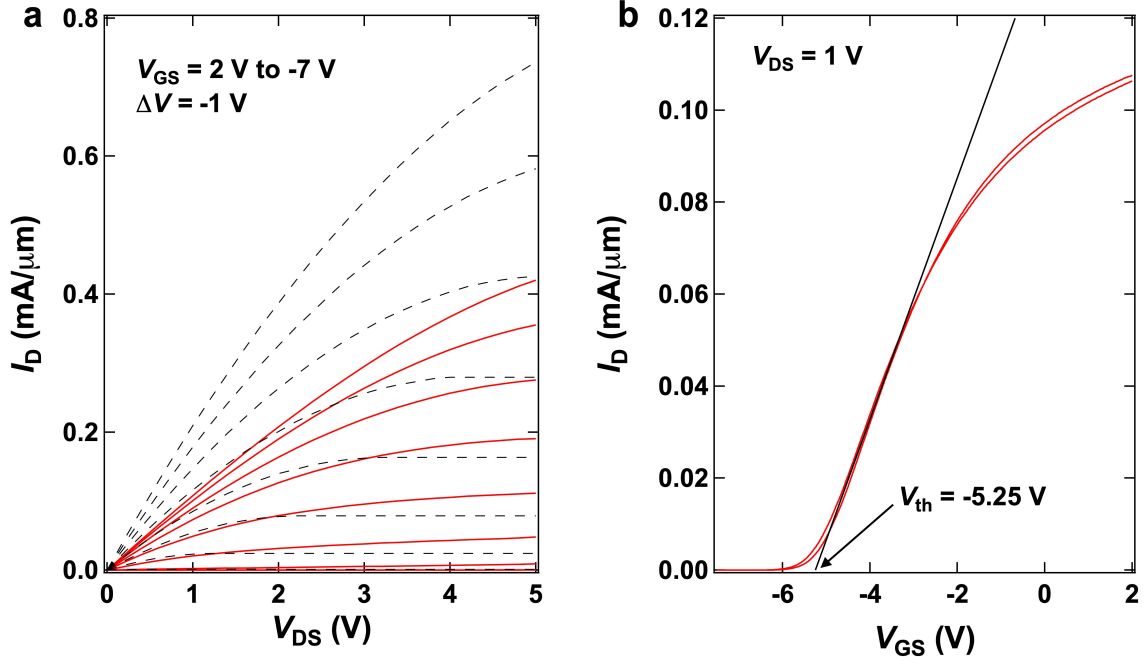
Supplementary Fig. 11. Simulation of the output characteristics of a BaSnO$_3$-based FET. (a) Comparison of the measured output characteristics with simulated output characteristics showing a slow increase of I_{DS} vs. V_{DS} due to the effect of a high contact resistance. (b) Extraction of the threshold voltage in the linear regime.

The simulated output characteristics are calculated using the Square-Law theory. The theoretical behavior is[S15]:

$$I_D = \frac{Z\mu_n C_0}{L}\left[(V_G - V_T)V_D - \frac{V_D^2}{2}\right] \begin{pmatrix} 0 \leq V_D \leq V_{Dsat} \\ V_G \geq V_T \end{pmatrix},$$

where

$$I_{Dsat} = \frac{Z\mu_n C_0}{L}\frac{(V_G - V_T)^2}{2} \quad (V_{Dsat} \leq V_D, V_{Dsat} = V_G - V_T).$$

Z, μ_n, C_0, and L are the channel width, effective mobility, capacitance per unit area of the gate dielectric, and channel length, respectively. The slower increase of I_{DS} vs. V_{DS} in the measured output characteristics than that of the simulated output characteristics is attributed to the high contact resistance of ITO as depicted with the dashed line in supplementary Fig. 8.

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