Electron Saturation Velocity Variation in InGaAs and GaAs Channel MODFET's for Gate Lengths to 550 Å

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Abstract—**MODFET's with InGaAs and GaAs channels have been fabricated with gate lengths between 2 μm and 550 Å and have been dc characterized at room temperature. An effective electron saturation velocity was calculated for each device from the peak transconductance. The GaAs channel devices show a peak in the transconductance and saturation velocity at a gate length of approximately 0.15 μm, while the transconductance and velocity of the InGaAs channel devices are nearly constant over the entire range of gate lengths.**

I. Introduction

THE MOST straightforward means to increase the high-frequency performance of MODFET's is to decrease the gate length and thus reduce the gate-source capacitance and increase the intrinsic transconductance. It is clear that improved performance can be realized by reducing the gate length to the order of 0.1 μm due to velocity overshoot effects in the MODFET, thus increasing the transconductance. A recent example of such work can be found in Chao *et al.* [1]. At some critical gate length, however, the transconductance values are expected to saturate, and no further improvement is to be expected [2]. In this work, both traditional GaAs channel MODFET's and InGaAs channel MODFET's with a spacer and a bottom electron confining layer were fabricated with gate lengths between 2 μm and 550 Å. These are the first experimental results comparing GaAs MODFET's and pseudomorphic confined channel MODFET's with gate lengths less than 0.1 μm.

II. Fabrication

Two wafers, each grown on a semi-insulating (100) GaAs substrate, were used in this study. A standard MODFET structure was grown on the first wafer by MBE consisting of a superlattice buffer layer (four layers each of 100-Å undoped $Al_{0.3}Ga_{0.7}As$ and 100 Å of GaAs), followed by a 4000-Å undoped GaAs buffer layer, a 300-Å $Al_{0.26}Ga_{0.74}As$ layer doped at 2×10^{18} cm^3 with Si, a graded Al composition layer of 150 Å doped at 4×10^{18} cm^3 followed by a 600 Å cap layer doped at 4×10^{18} cm^3 with Si. Upon the second wafer an InGaAs channel MODFET was grown, consisting of the same superlattice buffer layer, followed by a 2200-Å undoped GaAs buffer layer, a 120-Å $In_{0.15}Ga_{0.85}As$ undoped layer, a 20-Å undoped $Al_{0.21}Ga_{0.79}As$ spacer layer, a 500-Å $Al_{0.21}Ga_{0.79}As$ layer doped at 2×10^{18} cm^3, and a 600-Å GaAs cap layer doped at 4×10^{18} cm^3. Conceptual diagrams of both structures are shown in Fig. 1.

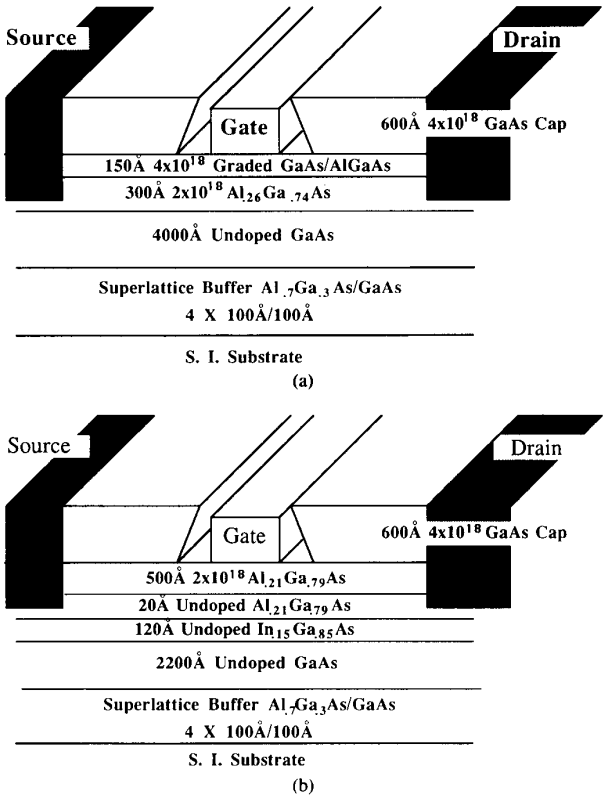

Fig. 1. Schematic diagram of the two MODFET structures fabricated: (a) GaAs channel MODFET, and (b) InGaAs channel MODFET.

After growth both wafers followed the same processing sequence. Using optical lithography and chemical etching,

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devices were first mesa isolated. Ohmic contacts were formed by depositing Ni/Au/Ge and annealing at 450°C for 30 s. 700-Å-thick PMMA in combination with an ultrahigh resolution electron-beam exposure system was used for defining the gate. Recess of the gate for all devices was accomplished by chemical etching using a citric acid:peroxide etch [3]. Gate metallization consisted of Ti/Al/Au totaling approximately 600 Å. Interconnect metallization was a thick Ti/Pt/Au. The processing details, including e-beam exposure system details, have been published previously [4]. Fig. 2(a) shows a SEM photograph of a completed device, with Fig. 2(b) showing the gate region of a 900-Å gate length device.

III. Results and Discussion

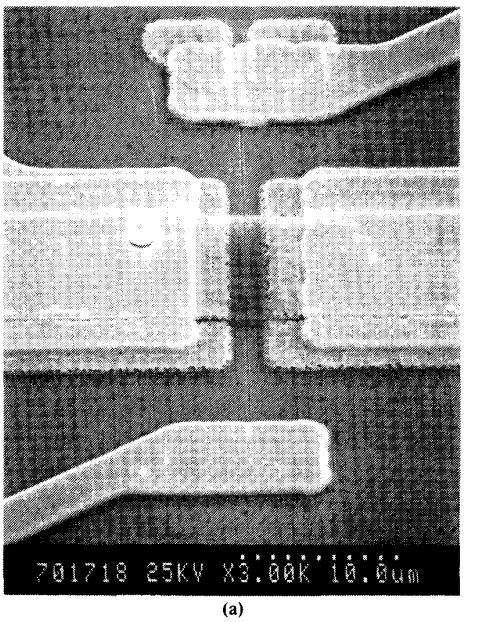
DC measurements on all MODFET devices were carried out. A typical I–V curve for a pseudomorphic device is shown in Fig. 3. In order to accurately determine the intrinsic transconductance and hence the saturation velocity of all devices, an accurate method of estimating the source resistance had to be used. Low field I–V measurements were taken in the range of 0- to 0.01-V source–drain bias within a range of gate biases. The source resistance was estimated from these measurements as half the maximum slope asymptotically approached for small forward bias voltages, and ranged from 50 to 140 Ω depending on the source–drain spacing of the device. Peak room-temperature extrinsic transconductances were measured for the conventional MODFET to be as high as 415 mS/mm. Room-temperature extrinsic transconductances reached 315 mS/mm for the pseudomorphic MODFET's. Output conductances were also measured in the region of the peak transconductance. From these measurements the intrinsic transconductance was found using the following equation [5]:

$$g_{mi}=\frac{g_m^0}{1-(R_S+R_D)g_{\text{out}}(1+R_S g_m^0)}$$

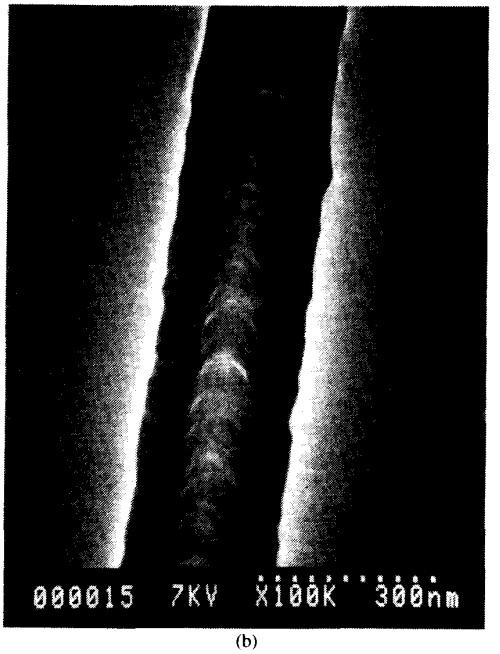
where

$$g_m^0=\frac{g_m}{1-R_S g_m}\,.$$

Comparison from device to device requires taking into account both etch depth differences, as well as contributions to the drain current from the parasitic MESFET [6], which can form under sufficiently positive gate bias near the region of peak transconductance. To alleviate these concerns the threshold voltage (V_{th}) was measured in the linear, very low field region with source–drain voltages (V_{ds}) of 0.01, 0.03, and 0.05 V. For each device, all linearly extrapolated V_{th} values for each V_{ds} agreed, assuring it is in a low enough field region that short-channel effects on the threshold voltage could be ignored. Devices with V_{th} much less than -1 V were ignored in the analysis. For the remaining depletion devices, the actual etch depth was determined by comparing the observed threshold voltage to that expected from a theoretical model of the conduction band for the device. Etch depth variation from device to device was found to be within a 100-Å range for similar type devices. This etch depth was then used to better determine d below.



(a)



(b)

Fig. 2. SEM photograph of a completed 900-Å gate length device: (a) low magnification view, and (b) close-up view showing width and recess into channel.

Assuming velocity saturation holds, to first order for small MODFET's, the peak intrinsic transconductance is given by

$$g_{m,\,\text{maximum}}=\frac{C_g}{\tau_d}=\frac{\epsilon Z v_s}{d+\Delta d}$$

where C_g is the gate capacitance (derivative of the electron sheet density versus gate voltage), τ_d is the transit time under the gate, ϵ is the dielectric constant, d is the distance between the gate and the channel, v_s is the "effective" saturation velocity, Z is the gate width, and Δd is the distance between

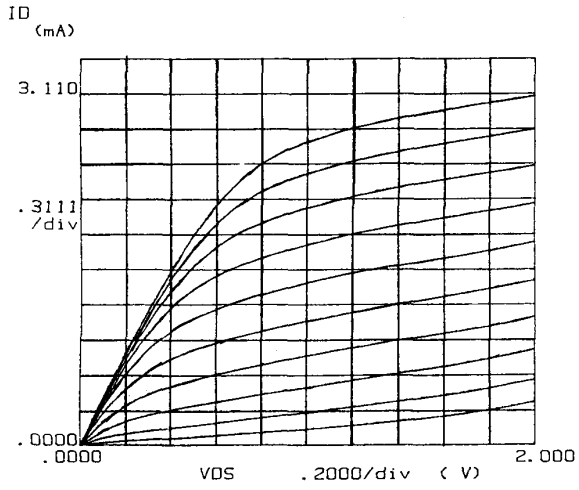


Fig. 3. Typical I-V curve for a completed pseudomorphic device. Gate voltages range from -0.4 to $+0.5$.

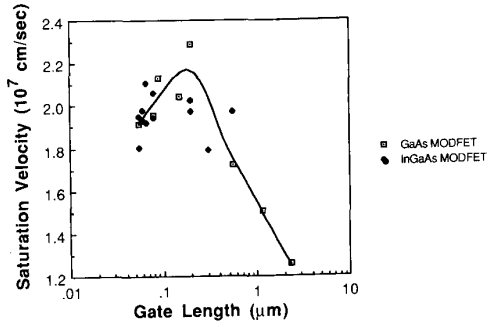


Fig. 4. Comparison of effective saturation velocities between the InGaAs channel and GaAs channel MODFET's. Note the peak that occurs only in the saturation velocity curve of the GaAs MODFET at a gate length of approximately 0.15 μm.

the peak or average of the electron wave function and the physical interface, which is approximately 80 Å [7], [8]. Using the etch depth found above, an "effective" saturation velocity was found for each device. This saturation velocity is a better figure for comparison than the peak transconductance due to the inclusion of etch depth differences. Fig. 4 shows this effective saturation velocity as a function of gate length for both GaAs channel devices and InGaAs channel devices.

The total length that the electrons must traverse in the saturated regime is, however, not exactly equal to the physical gate length for sufficiently small devices. The carrier transit time must be modified in a fashion similar to

$$\tau_d = \frac{L_g'}{v_s} = \frac{L_g + L_{gd}}{v_s}$$

where L_{gd} is the distance between the n^+ cap layer on the drain side and the gate [9]. The effect of this correction would be to raise the effective saturation velocity at the small gate-length end of the curve as the correction becomes more appreciable. However, the exact magnitude of this correction is unclear without extensive Monte Carlo simulations, although it would be expected to be of similar magnitude of both types of devices.

In the region of gate lengths down to about 0.2 μm, a higher degree of velocity overshoot effects are expected to increase the transconductance and the effective saturated electron velocity in the MODFET as the gate length is reduced [10]. This is observed prominently in the GaAs channel device. As the gate length is reduced even further, one sees a decrease in transconductance for the GaAs channel MODFET, which agrees with the prediction of Kizilyalli *et al.* [2] of a maximum transconductance at a gate length of about 0.15 μm. However, for the pseudomorphic MODFET, the saturation velocity is reasonably flat in this range. While more work is necessary to explain this result, tentative explanations might include such factors as a higher intervalley spacing for the InGaAs, and the further separation of the donors from the two-dimensional electron gas in the InGaAs structure.

IV. Summary

Traditional MODFET's and InGaAs channel MODFET's with a bottom electron confining layer were fabricated with gate lengths ranging from 2 μm to 550 Å. A peak in the transconductance and effective saturation velocity for the traditional MODFET was observed. However, virtually no dependence of gate length on transconductance was observed for the InGaAs confined channel device.

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