Patterning of sub-10-nm Ge islands on Si(100) by directed self-assembly

Olivier Guise, John T. Yates Jr., Jeremy Levy, Joachim Ahner, Venugopalan Vaithyanathan, and Darrell G. Schlom

Citation: Applied Physics Letters **87**, 171902 (2005); doi: 10.1063/1.2112198
View online: http://dx.doi.org/10.1063/1.2112198
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/87/17?ver=pdfcov
Published by the AIP Publishing

Patterning of sub-10-nm Ge islands on Si(100) by directed self-assembly

Olivier Guise, John T. Yates, Jr., and Jeremy Levy[a)]
University of Pittsburgh, Pittsburgh, Pennsylvania 15260

Joachim Ahner
Seagate Technology, Pittsburgh, Pennsylvania 15222

Venugopalan Vaithyanathan and Darrell G. Schlom
Pennsylvania State University, University Park, Pennsylvania 16802

(Received 28 April 2005; accepted 14 September 2005; published online 17 October 2005)

A process is reported for creating arbitrary patterns of sub-10-nm Ge islands on a Si(100) substrate by directed self-assembly. Carbon-based templates are created on Si substrates by electron-beam-induced deposition using high-resolution electron beam lithography. Ozone etching, followed by annealing in ultra-high vacuum, yields small (<4 nm) SiC nucleation sites for subsequently deposited Ge. Quantitative analysis of atomic force microscope images reveals templated Ge islands with mean diameter $d \sim 8$ nm, averaging 2000 ± 500 atoms per island, with controlled spacings as small as 35 nm, and 2 nm absolute positional accuracy. The Ge/Si nanostructures reported here may find use in end-of-scaling classical computing and single-electron devices and spin-based quantum computing architectures. © *2005 American Institute of Physics*.
[DOI: 10.1063/1.2112198]

Silicon-based devices with feature sizes at and below 10 nm represent the final stage for Moore's law scaling.[1] At these length scales, quantum confinement, tunnelling, and charge quantization can disrupt the functionality of conventional devices. These same quantum effects are essential for the operation of room-temperature single electron transistors,[2–5] quantum cellular automata,[6] and proposed Si-based quantum computing architectures.[7–10] Here we present a method for patterning sub-10-nm Ge nanostructures on Si(100) using a novel process of directed self-assembly. Electron-beam-induced decomposition of carbon-containing molecules on a silicon substrate produces carbon clusters that upon annealing in ultra-high-vacuum (UHV) form stable SiC nucleation sites. Subsequent deposition of Ge leads to templated growth of sub-10-nm Ge islands. We demonstrate control over Ge island size and placement that are significantly beyond what has been achieved previously. These nanostructured materials form attractive candidates for producing quantum devices that can operate at room temperature.

Two important parameters related to the patterning of Ge nanoscale islands on Si are their average size D and spacing L. Nanoscale Ge islands ($D \sim 20$–100 nm) can be created on Si(100) via the Stranski–Krastanov instability, in which three-dimensional Ge islands form over a two-dimensional wetting layer that exceeds a critical thickness.[11–13] The kinetic and thermodynamic constraints on Ge island growth[12,14–16] produce random arrangements of islands with average diameters $D \geqslant 20$ nm and separations $L \geqslant 50$ nm. Pre-adsorption of carbon precursors [typically ~0.1 monolayer (ML)] has been shown to produce smaller ($D \sim 10$ nm) Ge islands on Si(100).[17] The islands are also randomly distributed, with a high density ($\sim 10^{11}/\mathrm{cm}^2$) and relatively narrow size distribution.

To control the placement of individual islands, several groups have developed templates using lithographic patterning[18–20] or focused ion beam implantation.[21] In all cases, the smallest island size that has been achieved is $D \sim 40$ nm, and the smallest separation observed is $L \sim 80$ nm.

Our approach to creating precise patterns of Ge islands (Fig. 1) exploits the ability of carbon to template the growth of Ge islands on Si(100). Single-side polished 2″ diameter Si(100) substrates (phosphorus-doped, resistivity $\rho \sim 10^{-2}\Omega$ −cm) are first treated with ozone and then chemically cleaned using standard methods,[22] leading to the formation of a smooth hydrogen-passivated Si surface [RMS <3 Å over a 1 μm scan size, measured by atomic-force microscopy (AFM)]. A high-resolution electron-beam lithography system [Fig. 1(a)] exposes this surface to a focused

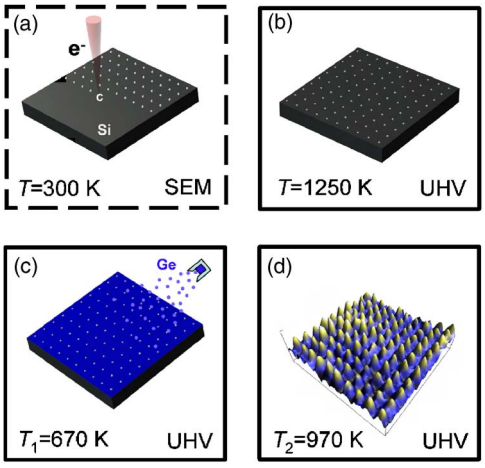

FIG. 1. Schematic for templated Ge island growth. (a) Electron-beam induced deposition of carbon dot template; (b) annealing in ultra-high vacuum to form SiC nucleation sites; (c) deposition of Ge at temperature T_1; (d) AFM image (350 nm × 350 nm × 2 nm) of Ge islands that form after annealing at temperature T_2.

[a)]Electronic mail: jlevy@pitt.edu

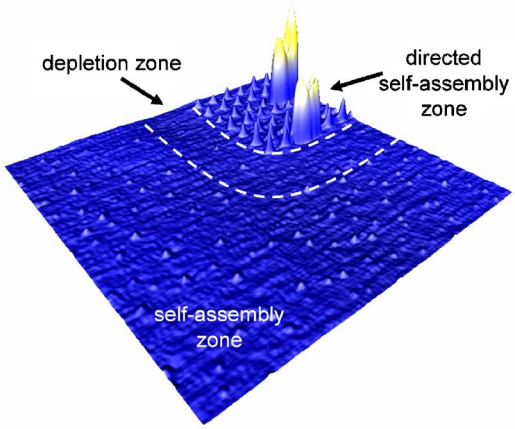

FIG. 2. AFM image (5 μm$\times$5 μm$\times$35 nm) showing co-existence of self-assembled and templated Ge islands.

($\sim$1 nm) beam of electrons (340 pA, 20 keV). Ambient carbon-containing molecules decompose on the surface, forming "carbon dots" whose diameters $d\sim$4–10 nm and heights $h\sim$1–10 nm depend on the electron beam exposure time per dot t_{el} (typically 10^{-4}–10^{-1} s). Details about the carbon templating procedure are described elsewhere.[23]

After patterning, the Si wafer is again treated with ozone. This second exposure reduces the size of the carbon dots, removes hydrocarbons decomposed by secondary electrons during exposure, and creates a protective oxide surface layer[24] that can be subsequently removed in UHV. The ozone exposure time should be longer than the time required to remove the background adsorbed hydrocarbons, and shorter than the time required to completely remove the carbon dots.

The patterned Si wafer is transferred to a UHV molecular-beam epitaxy (MBE) system and radiatively heated to T_0=1250 K for $\sim$5 min [Fig. 1(b)]. This step removes the protective oxide layer, and causes the carbon islands to react with Si to form highly stable SiC nucleation sites.[25] The sample temperature is then reduced to T_1 (typically 670 K) over 30 min, and $N_{Ge}\sim$1–2 ML of Ge (where 1 ML=678 atoms/100 nm^2) are deposited from an effusion cell onto the substrate at a rate R=0.06 Å/s [Fig. 1(c)]. The base pressure in the MBE chamber is typically 1–2 $\times10^{-9}$ mbar, and no higher than 5×10^{-9} mbar during Ge growth. After Ge deposition, the sample is usually post-annealed at T_2 (typically 970 K) for a time t_2 (typically 30 min) to produce patterned islands. This last step greatly increases the surface mobility of Ge adatoms and is responsible for the formation of islands. Figure 1(d) shows an AFM image of a pattern of Ge islands created using this method (details are discussed below with Fig. 4).

Throughout the MBE growth process (annealing, Ge deposition, post-annealing), the quality of the surface is monitored by reflection high-energy electron diffraction (RHEED) to ensure complete removal of the oxide layer prior to Ge-deposition. Because of the small number of patterned carbon dots created in a typical experiment ($\sim10^6$), neither the SiC nor the surface roughness due to templated Ge growth are detectable by RHEED.

Figure 2 provides direct evidence that the SiC dots form attractive sites for mobile Ge adatoms. In this experiment, a 25$\times$25 square array of SiC dots is prepared (t_{el}=100 ms, corresponding to a dot diameter $\sim$30 nm, height $\sim$10 nm before ozone treatment and annealing). The AFM image shows one corner of the array; the rest of the region is unpatterned. Deposition of 4 ML of Ge at R=0.06 Å/s and $T_1=T_2$=850 K (i.e., no distinct post-deposition annealing step) produces both self-assembled and patterned Ge islands. Two relatively large Ge islands have formed over neighboring pairs of SiC dots, illustrating strong wetting of Ge on the patterned areas. Near the array boundary, the density of self-assembled islands falls significantly, indicating that the wetting layer thickness on the Si is locally reduced. An analysis of the spatial distribution of self-assembled Ge islands confirms that this depletion region begins $\sim$2 μm from the edge of the array. These diffusion lengths are consistent with other reported values for the annealing conditions used here.[26] No self-assembled islands are observed between the patterned islands, indicating that the Ge wetting layer thickness is reduced in the region between the patterned islands as well.

Further experiments are performed to determine the influence of various growth parameters such as the electron-beam exposure time t_{el}, ozone-treatment duration prior to UHV-transfer, amount of Ge deposited, Ge deposition rate and temperature, and post-deposition annealing conditions. Figure 3 shows the result of a pattern formed with t_{el} =18 ms exposures, followed by deposition of 2 ML of Ge at a rate R=0.06 Å/s, at a temperature where the Ge is highly mobile ($T_1=T_2$=830 K). The AFM image [Fig. 3(a)] shows an irregular distribution of volumes; 99% of the observed islands exist on lattice sites defined by the SiC pattern, as

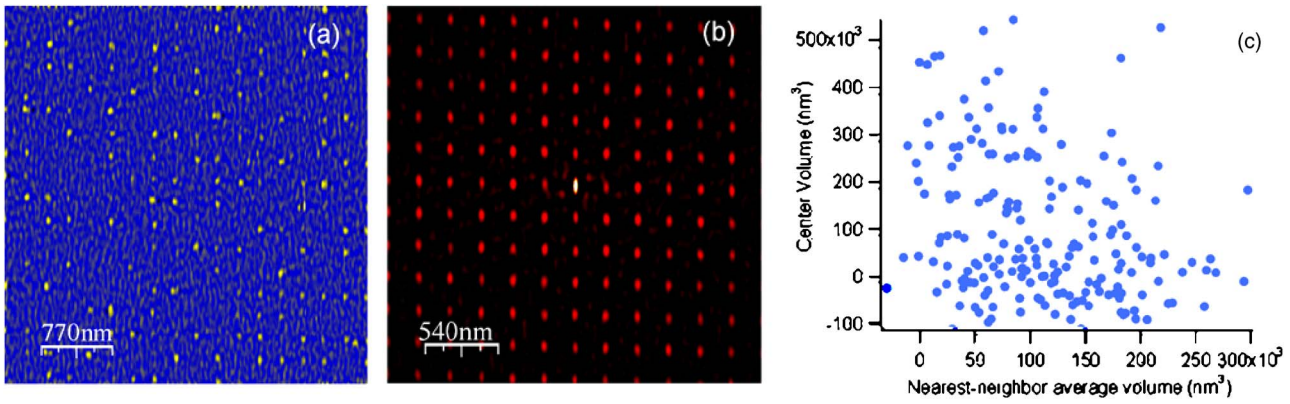

FIG. 3. Templated Ge islands grown at $T_1=T_2$=830 K. (a) AFM image of templated region; (b) autocorrelation of AFM image, showing expected periodicity; (c) scatter plot of island volume versus average nearest neighbotr volume. The estimated margin of error in determining island volumes is indicated by the shaded region, and the dashed line is a guide for the eye.

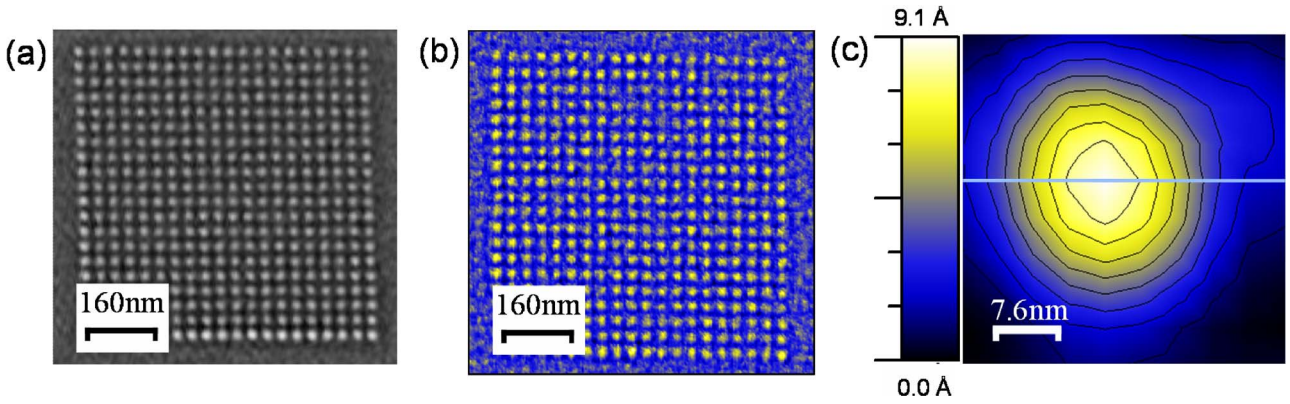

FIG. 4. (a) AFM image of 20×20 array of SiC dots; (b) AFM image of 20×20 array of Ge islands on SiC template; (c) average topographic profile of 400 Ge islands. Contours are separated by 1Å.

evidenced by an autocorrelation of the AFM image [Fig. 3(b)]. The distribution of island volumes resembles those reported for self-assembled Ge islands on untemplated surfaces.[12,14–16] Correlations between the sizes of the Ge islands are revealed by comparing the volume of a given island with that of its four nearest neighbors [Fig. 3(c)]. Larger islands exhibit a clear tendency to have smaller (and fewer) neighbors.

Separating the Ge deposition and annealing steps greatly sharpens the distribution of island sizes. Fig. 4(a) shows a 20×20 array of carbon dots spaced by 35 nm ($t_{el}=1$ ms) and the resulting Ge islands [Fig. 4(b)] grown under the following conditions: $N_{Ge}=1$ ML at $R=0.06$ Å/s, $T_1=670$ K; annealed at $T_2=970$ K for $t_2=30$ min. Except for isolated defects, no islands are observed in untemplated areas, i.e., outside the array or in interstitial regions.The averaged profile of the 400 islands [Fig. 4(c)] is Gaussian: $z(x)=h\exp(-(x/\sigma)^2)$, with $h=9.2$ Å and $\sigma=12.4$ nm. Assuming a 4 nm radius of curvature for the noncontact Si probe,[23] and taking into account the 2 nm spatial variations in the absolute registry of the islands, one obtains $\sigma'\approx6$ nm for the islands, corresponding to a full-width half-maximum (FWHM) $d\approx8$ nm. Each island contains $\sim2000\pm500$ Ge atoms. Fluctuations are large, the result of unavoidable statistical fluctuations as well as competition for Ge by nearest neighbors, i.e., Oswald ripening. An analysis of the spatial location of the patterned islands shows that the islands form within 2 nm of their intended location.

More experimental and theoretical work is required to understand the ultimate level of control with which Ge nanostructures can be created on Si(100) using the methods presented here. To become useful for quantum device architectures, it will be important to understand how Ge adatoms bond with the SiC sites, how the kinetic history of the Ge can be tailored to reduce island size fluctuations, and how their structure relates to electronic and optical properties. The sub-10-nm Ge islands demonstrated here are already interesting for quantum devices that work with single electrons and holes. Single-electron charging energies for sub-10-nm Ge islands exceed thermal energies,[4] raising the prospect of creating single-electron transistors that operate at room temperature. The high precision with which the islands can be placed is critical for the engineering of dipolar and tunnel couplings for quantum cellular automata and quantum computing device architectures.

This work was supported by the DARPA QuIST program (DAAD-19-01-1-0650).

[1]M. Ieong, B. Doris, J. Kedzierski, K. Rim, and M. Yang, Science **306**, 2047 (2004).
[2]L. Guo, E. Leobandung, and S. Y. Chou, Science **275**, 649 (1997).
[3]S. J. Tans, A. R. M. Verschueren, and C. Dekker, Nature (London) **393**, 49 (1998).
[4]S. Y. Huang, S. Banerjee, R. T. Tung, and S. Oda, J. Appl. Phys. **94**, 7261 (2003).
[5]P. W. Li, W. M. Liao, D. M. T. Kuo, S. W. Lin, P. S. Chen, S. C. Lu, and M. J. Tsai, Appl. Phys. Lett. **85**, 1532 (2004).
[6]C. S. Lent, P. D. Tougaw, and W. Porod, Appl. Phys. Lett. **62**, 714 (1993).
[7]B. E. Kane, Nature (London) **393**, 133 (1998).
[8]J. Levy, Phys. Rev. A **64**, 052306 (2001).
[9]T. D. Ladd, J. R. Goldman, F. Yamaguchi, Y. Yamamoto, E. Abe, and K. M. Itoh, Phys. Rev. Lett. **89**, 017901 (2002).
[10]M. Friesen, P. Rugheimer, D. E. Savage, M. G. Lagally, D. W. van der Weide, R. Joynt, and M. A. Eriksson, Phys. Rev. B **67**, 121301 (2003).
[11]I. N. Stranski and L. Krastanow, Akad. Wiss. Lit. Mainz Abh. Math. Naturwiss. Kl. **146**, 797 (1939).
[12]Y.-W. Mo, D. E. Savage, B. S. Swartzentruber, and M. G. Lagally, Phys. Rev. Lett. **65**, 1020 (1990).
[13]D. J Eaglesham and M. Cerullo, Phys. Rev. Lett. **64**, 1943 (1990).
[14]J. Drucker and S. Chaparro, Appl. Phys. Lett. **71**, 614 (1997).
[15]G. Medeiros-Ribeiro, A. M. Bratkovski, T. I. Kamins, D. A. A. Ohlberg, and R. S. Williams, Science **279**, 353 (1998).
[16]F. M. Ross, R. M. Tromp, and M. C. Reuter, Science **286**, 1931 (1999).
[17]O. G. Schmidt, C. Lange, K. Eberl, O. Kienzle, and F. Ernst, Thin Solid Films **321**, 70 (1998).
[18]L. H. Nguyen, V. LeThanh, D. Debarre, V. Yam, M. Halbwax, M. El Kurdi, D. Bouchier, P. Rosner, M. Becker, M. Benamara, and H. P. Strunk, Appl. Surf. Sci. **224**, 134 (2004).
[19]E. S. Kim, N. Usami, and Y. Shiraki, Appl. Phys. Lett. **72**, 1617 (1998).
[20]G. Jin, J. L. Liu, and K. L. Wang, Thin Solid Films **369**, 49 (2000).
[21]M. Kammler, R. Hull, M. C. Reuter, and F. M. Ross, Appl. Phys. Lett. **82**, 1093 (2003).
[22]W. Kern, *Handbook of Semiconductor Wafer Cleaning Technology—Science, Technology and Applications* (Noyes/William Andrew, Norwich, NY, 1993).
[23]O. Guise, J. Ahner, J. T. Yates, Jr., and J. Levy, Appl. Phys. Lett. **85**, 2352 (2004).
[24]J. R. Vig, J. Vac. Sci. Technol. A **3**, 1027 (1985).
[25]O. Guise, H. Marbach, J. Levy, J. Ahner, and J. T. Yates Jr., Surf. Sci. **571**, 128 (2004).
[26]Y. Suda, S. Kaechi, D. Kitayama, and T. Yoshizawa, Thin Solid Films **464-65**, 190 (2004).