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Annealing condition optimization and electrical characterization of amorphous $LaAlO_3$/GaAs metal-oxide-semiconductor capacitors

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The electrical properties of amorphous $LaAlO_3$/GaAs metal-oxide-semiconductor capacitors fabricated using molecular-beam deposition are investigated. The surface was protected during sample transfer between III-V and oxide molecular beam epitaxy chambers by a thick arsenic-capping layer. Amorphous $LaAlO_3$ was deposited on $c(4\times4)$ and (2×4) reconstructed (100) GaAs surfaces. An annealing method, a low temperature-short time rapid thermal annealing (RTA) followed by a high temperature RTA, was developed, yielding extremely small hysteresis (~30 mV), frequency dispersion (~60 mV), and interfacial trap density (mid-10^{10} eV^{-1} cm^{-2}).
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One of the approaches to realize low power and high-speed/frequency devices is to use materials in which the carrier mobility is much higher than that of silicon, such as gallium arsenide (GaAs) or indium gallium arsenide (InGaAs). For the past 30 years, the lack of a useful surface passivation for compound semiconductors has, however, precluded development of metal-oxide-semiconductor (MOS) devices and caused high surface recombination parasitics in scaled devices. Oxidation and metal deposition on III-V materials create a high interface trap density (D_{it}), the former by causing considerable local lattice rearrangement and the latter by disturbing the periodic structure at the surface.[1,2] Extra metallic arsenic (As) atoms on the surface also lead to high D_{it}.[3] The high trap density due to surface/interface defects pins the Fermi level near the energy band gap center, which prevents modulation of the surface potential with gate bias voltage in the case of a metal-oxide-semiconductor field-effect transistor.

The development of high performance GaAs-based MOS device applications demands proper surface treatment techniques and interfaces to reduce D_{it}. In addition, a high dielectric constant material is essential to decrease the gate leakage current and enables the continuation of MOS scaling. Many insulators, such as Si_3N_4, $Ga_2O_3(Gd_2O_3)$,[4] Al_2O_3,[5] and HfO_2 (Ref. 6) are currently being explored. Amorphous $LaAlO_3$ on Si has shown good thermal stability, a high optical band gap (6.2 eV for amorphous $LaAlO_3$) and a high dielectric constant [16±2 for amorphous $LaAlO_3$ films deposited by molecular-beam deposition (MBD)].[7,8]

In previous work, we illustrated what types of annealing effectively improved the interface quality of amorphous $LaAlO_3$ deposited on the $c(4\times4)$ and (2×4) surface reconstructions of (100) GaAs.[9] Here, we introduce an optimized annealing process using a two-step annealing method that significantly reduces *C-V* hysetersis, frequency dispersion, and D_{it}. We characterize the interface using capacitance-voltage (*C-V*), current-voltage (*I-V*), and conductance-voltage (*G-V*) measurements.

After *in situ* desorption of its native oxide, a Be doped [$(1\pm0.5)\times10^{18}$ cm^{-3}] 300 nm epitaxial GaAs layer was grown at 580 °C on *p*+ GaAs (100) substrate [Zn doping of $(0.5–5)\times10^{19}$ cm^{-3}] in a Varian Gen II ultrahigh vacuum (UHV) molecular-beam epitaxy system. A thick amorphous arsenic (As) capping layer was deposited after GaAs growth using an As_2 flux (the As beam equivalent pressure $=2.5\times10^{-6}$ Torr) at room temperature for 1 h. The As capping layer efficiently protects the GaAs surface from oxidation and contamination during wafer transfer. The sample was transferred in air to the MBD chamber for $LaAlO_3$ deposition. An *in situ* reflection high-energy electron diffraction (RHEED) system was used to monitor the surface reconstruction pattern as the As capping layer was thermally desorbed.[10] Two types of surface conditions were achieved by heating in ultrahigh vacuum: an As-rich $c(4\times4)$ surface at 325 °C and an As-stabilized (2×4) surface at 480 °C. These RHEED patterns suggest that there are more free As atoms at the interface of the $c(4\times4)$ sample than of the (2×4) sample.[10–12] After cooling the samples in UHV to 80 °C, a 10 nm amorphous $LaAlO_3$ film was deposited using elemental lanthanum, aluminum, and oxygen sources.[7,8] After removal from MBD system and air exposure, a 100 nm thick of Al film was evaporated by *e* beam on the sample through a shadow mask to form the gate electrodes. The back side Ohmic contact was formed using a composite stack of 50 nm of titanium (Ti) followed by 150 nm of gold (Au).

First, we investigated the effect of forming gas furnace annealings (FGAs) (4% hydrogen and 96% N_2) on the $c(4\times4)$ sample. To avoid the diffusion of arsenic atoms from the GaAs surface into the $LaAlO_3$ layer, low temperature (≤300 °C) and long time FGAs were executed; (i) at 295 °C for 80 or 85 min, (ii) at 285 °C for 85 or 95 min.

Second, we developed a two-step annealing method for the $LaAlO_3$ on (2×4) reconstructed samples to decrease the *C-V* hysteresis and frequency dispersion at the same time. Based on the assumption that the *C-V* hysteresis is caused by

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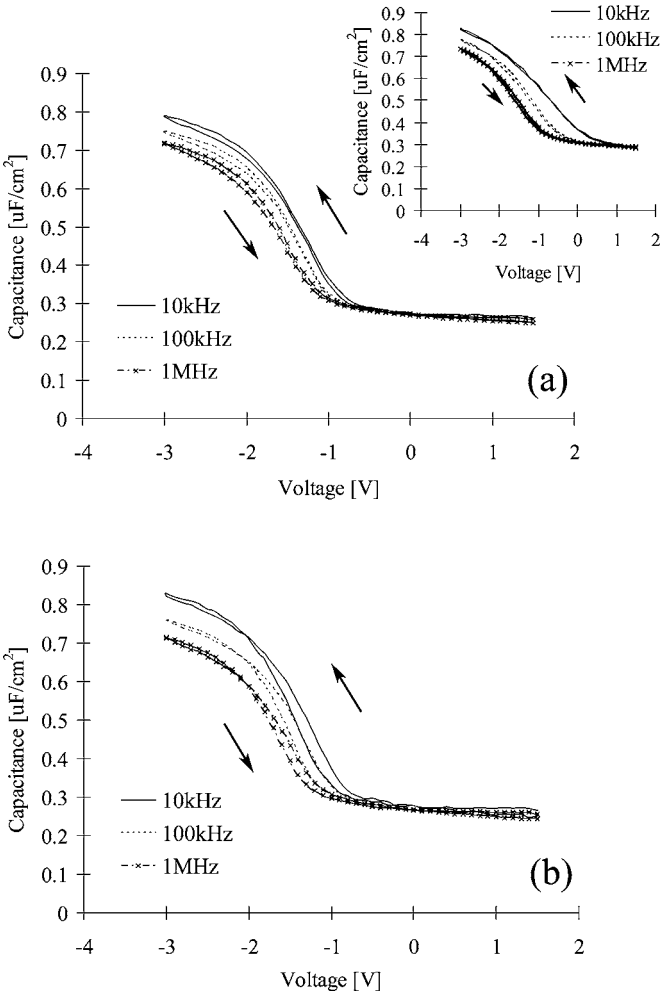

FIG. 1. *C-V* characteristics of a $LaAlO_3/c(4\times4)$ sample annealed at (a) 295 °C, 80 min FGA and (b) 295 °C, 85 min FGA. The inset of (a) shows the as-deposited $c(4\times4)$ sample *C-V* curves.

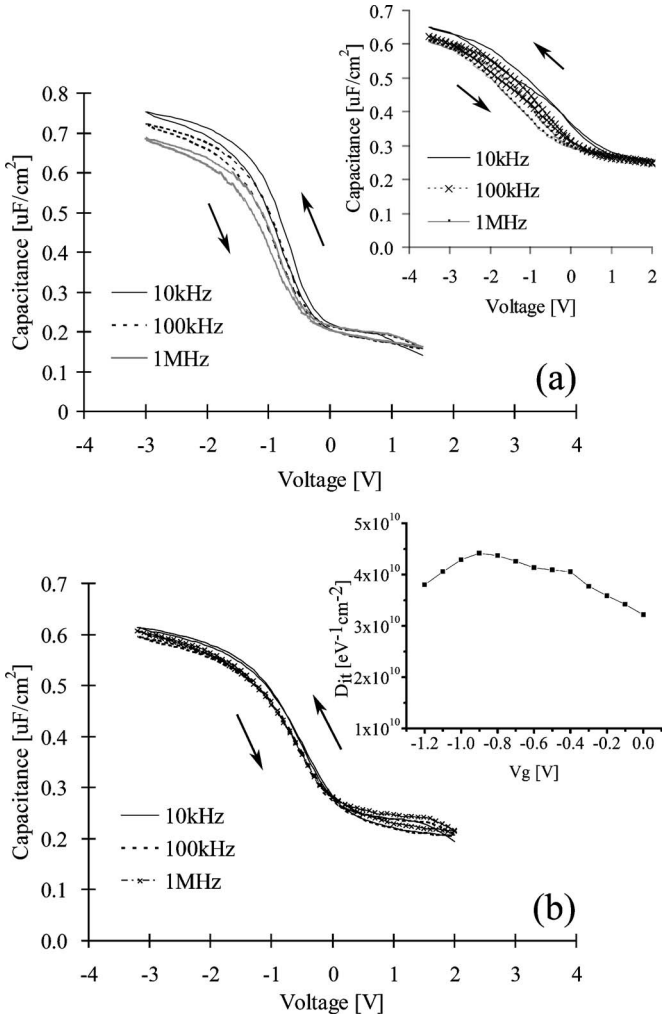

FIG. 2. *C-V* characteristics of a $LaAlO_3/(2\times4)$ sample annealed by (a) single post-metal- deposition RTA at 450 °C for 2 min in N_2 and (b) the LSHT RTA. The insets show (a) *C-V* curves of the as-deposited (2×4) sample and (b) the D_{it} measured using the high frequency conductance method.

As diffusion from the GaAs surface into the oxide, a low temperature (<300 °C) short time (<10 s) rapid thermal annealing (RTA) in N_2 was performed first to anneal the $LaAlO_3$ layer without As diffusion. This was followed by a normal high temperature RTA at 450 °C for 2 min in N_2. For the purpose of this discussion, this method will be called a low temperature spike RTA followed by a high temperature RTA (LSHT RTA) method. For comparison, a single high temperature RTA at 450 °C for 2 min in N_2 was executed after deposition of the Al gate electrodes. The *C-V* measurements were performed at frequencies of 10 kHz, 100 kHz, and 1 MHz in a shielded probe station at room temperature in the dark using an Agilent 4284A Precision *LCR* meter.

Figure 1 shows the *C-V* measurements of $LaAlO_3/c(4\times4)$ samples. The inset of Fig. 1(a) depicts *C-V* curves for an as-deposited samples which show small hysteresis (~60 mV), but large frequency dispersion (~430 mV). This indicates the presence of a substantial interface trap capacitance due to a large D_{it}. A 295 °C, 80 min FGA significantly reduced the frequency dispersion (100–150 mV) while still maintaining the small hysteresis (~60 mV) [Fig. 1(a)]. The hysteresis emerged when a sample was annealed only 5 min longer at the same temperature in Fig. 1(b). No additional improvement was achieved due to the limitation of the arsenic rich $c(4\times4)$ starting surface.

The *C-V* characteristics of $LaAlO_3/(2\times4)$ surface reconstruction samples are illustrated in Fig. 2. A single post-metal-deposition RTA at 450 °C for 2 min in N_2 appears to reduce the *C-V* hysteresis (~190 mV) and frequency dispersion (~180 mV) [Fig. 2(a)]. However, as shown in Fig. 2(b), the LSHT RTA method significantly eliminates these undesirable problems, resulting in a *C-V* hysteresis of ~30 mV, no frequency dispersion between 100 kHz and 1 MHz, and 60 mV frequency dispersion between 10 kHz and 100 kHz. The *C-V* curves exhibited little change between unannealed and just a low temperature–spike RTA (LS RTA). The two-step LSHT RTA method, however, produced *C-V* curves with little hysteresis; a range of 255–275 °C temperature and 10–20 s duration LS RTA followed by a 450 °C, 2 min RTA produced the best results. The inset of Fig. 2(b) shows the D_{it} to be below 5×10^{10} eV^{-1} cm^{-2} around midgap measured using the high frequency conductance method.[13] The *G-V* curves were corrected for series resistance. Then peak values of $G_P(\omega)/\omega$ curves were measured for the D_{it} calculation.[13] The *C-V* curves and D_{it} for this process are comparable to those of $Ga_2O_3(Gd_2O_3)$.[4] When samples were annealed at too high a temperature or for too long a time, the hysteresis increased again. Based on this result, we speculate that the

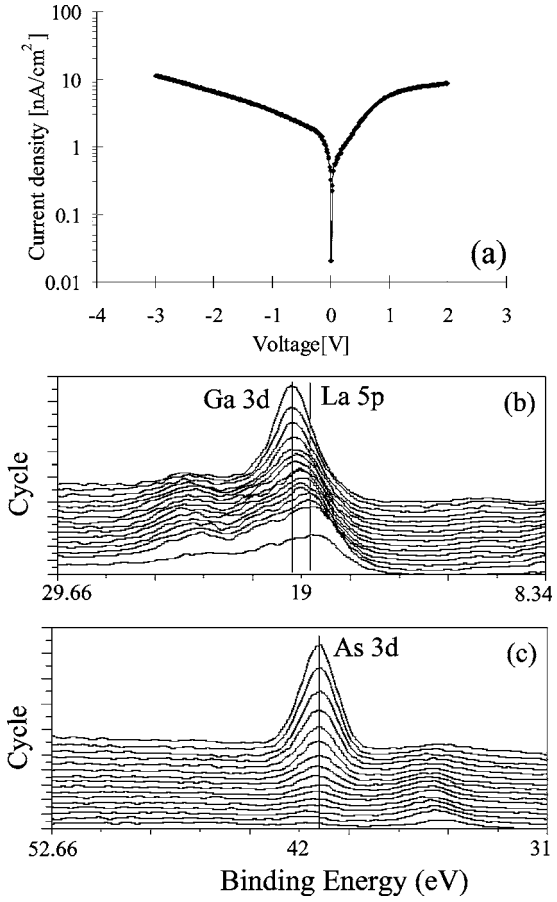

FIG. 3. (a) Leakage current density of the $LaAlO_3/(2\times4)$ sample shown in Fig. 2(b) (after LSHT RTA). The interfacial depth profiles of (b) Ga 3*d* and (c) As 3*d* core level of the same sample treated using the LSHT RTA method.

first LS RTA might anneal and densify the $LaAlO_3$ layer, which then impedes any subsequent As diffusion and charge trapping in the oxide. The second high temperature RTA then anneals the interface and rearranges the As atoms, resulting in a low D_{it}. Further experiments are in progress to analyze the LSHT RTA effect. In Fig. 3(a), low gate leakage current is also maintained after these annealings. Figure 3(b) and 3(c) illustrate the interfacial depth profile of Ga and As 3*d* core levels of a LSHT RTA sample measured by x-ray photoelectron spectroscopy. It reveals no As_2O_3 or Ga_2O_3 either at the interface or in the oxide.

In summary, we have optimized the annealing condition for $LaAlO_3$/GaAs MOS capacitors. The GaAs surfaces were protected by a thick As cap layer during sample transfer, which was subsequently desorbed under UHV prior to the $LaAlO_3$ deposition. The annealing effects on the two differently reconstructed GaAs surfaces illustrate the relationships between the starting surface condition and the resultant interface trap density level. The As-rich $c(4\times4)$ surface led to a larger frequency dispersion in the *C-V* characteristics, which is most likely due to a high interface trap density. Most importantly, the LSHT RTA method efficiently reduces the D_{it}, the bidirectional *C-V* hysteresis, and frequency dispersion, while still maintaining a reasonable leakage current level. MOS transistor fabrication and similar characterization of *n*-type samples are in progress.

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