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High-indium-content InGaAs metal-oxide-semiconductor capacitor with amorphous $LaAlO_3$ gate dielectric

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The structure and electrical properties of $LaAlO_3/n\text{-}In_{0.53}Ga_{0.47}As$ metal-oxide-semiconductor capacitors deposited by molecular-beam epitaxy were investigated. Transmission electron microscopy revealed a sharp interface between the dielectric and InGaAs. Postdeposition annealing at 440–500 °C significantly reduced the capacitive equivalent thickness and frequency dispersion. A hysteresis of 15 mV–0.1 V, a dielectric permittivity of 17 ± 1, and a dielectric strength of ~4.3 MV/cm were measured. Additionally, a high loss in the parallel conductance and gate-bias independence in the inversion region was observed, implying the fast generation rate of minority carriers in $In_{0.53}Ga_{0.47}As$. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2776846]

Due to limits to scaling of silicon, the use of alternative III-V compound semiconductor channels such as $In_{\geqslant 0.53}Ga_{\leqslant 0.47}As$ and InSb in complementary metal-oxide-semiconductor (MOS) devices is becoming attractive due to their higher electron mobilities and smaller band gaps.[1–3] It is surmised that integration of a high quality gate dielectric may help reduce gate leakage and improve I_{on}/I_{off} ratio in such devices. Recently $In_{<0.3}Ga_{>0.7}As$ devices with various high dielectric constant (high-κ) insulators showing superior electrical properties have been demonstrated.[4–6] In this letter we describe the physical and electrical characteristics of thin amorphous lanthanum aluminate ($LaAlO_3$) deposited on $In_{0.53}Ga_{0.47}As$.

Silicon-doped $In_{0.53}Ga_{0.47}As$ layers were grown on (001) InP substrates in a GEN II molecular-beam epitaxy (MBE) system at the University of Oklahoma. To minimize the dielectric/III-V layer interface defect density, the InGaAs samples were capped with arsenic[7] and shipped in a vacuum container to Penn State University. The cap was desorbed in a Veeco 930 MBE system in the absence of arsenic overpressure. Amorphous $LaAlO_3$ was then deposited as described elsewhere.[8–14] Reflection high-energy electron diffraction showed the $LaAlO_3$ to be amorphous. Tungsten (W) was evaporated *ex situ* either on as-deposited or postdeposition annealed (PDA) dielectric film to form the gate electrode and subsequently a MOS capacitor (MOSCAP). Evaporated indium or Ni–Ge–Au alloy formed Ohmic contact.

The structural integrity, dielectric physical thickness ($t_{oxide,}$) and electrical characteristics in MOSCAPs were determined by cross-sectional high-resolution transmission electron microscopy (HRTEM), spectroscopic ellipsometry, capacitance-voltage (C-V), and current density–voltage (J-V) measurements. The $LaAlO_3$ film stoichiometry was established by medium energy ion scattering (MEIS) technique and Rutherford backscattering spectrometry.[10,11]

The absence of an interfacial layer (IL) between amorphous $LaAlO_3/Si$ has been previously noted.[12] A comprehensive thermodynamic analysis of the stability of binary oxides in contact with III-V semiconductors[15] indicates no expected reactions between La_2O_3 or Al_2O_3 with GaAs or InAs and thus from a zeroth-order bond strength argument, $LaAlO_3$ is expected to be stable in contact with InGaAs. HRTEM image (Fig. 1) shows no distinct IL between $InGaAs/LaAlO_3/W$ interfaces following a 500 °C PDA (or 440 °C, not shown)

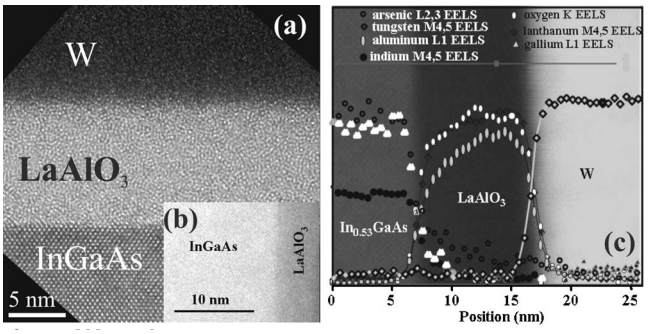

FIG. 1. (a) HRTEM image of a $W/LaAlO_3/n\text{-}In_{0.53}Ga_{0.47}As$ MOS capacitor after a PDA in a nitrogen ambient at 500 °C (5 min). As-deposited (not shown) and annealed (at 440 or 500 °C) $LaAlO_3$ are amorphous. (b) High angle annular dark-field scanning TEM (HAADF-STEM) reveals an abrupt interface between the $LaAlO_3$ and InGaAs. (c) The cross-sectional composition information as obtained by electron energy loss spectroscopy (EELS) and energy dispersive x-ray spectroscopy is overlayed on the HAADF-STEM micrograph of the sample. Humps seen in the dielectric film composition are an artifact of the nonuniformity of the sample thickness in cross section.

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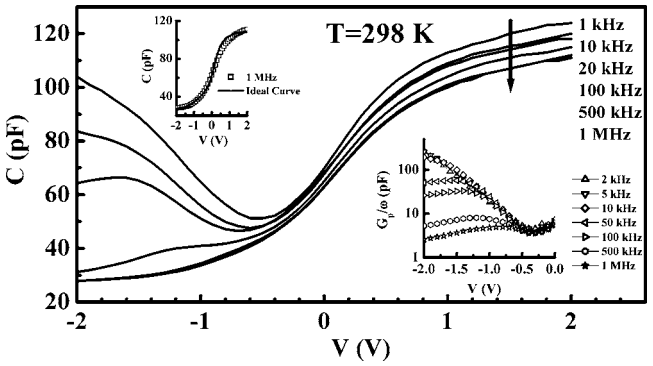

FIG. 2. As measured room temperature multifrequency capacitance as a function of applied gate voltage (V) for a W/$LaAlO_3$/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor with an area of 7.85×10^{-5} cm^2, following PDA at 500 °C in an N_2 ambient. The upper inset shows a comparison between the ideal C-V behavior and that measured at 1 MHz. The lower inset shows G_p/ω (log scale)-V, where G_p is parallel conductance and ω is the measured angular frequency.

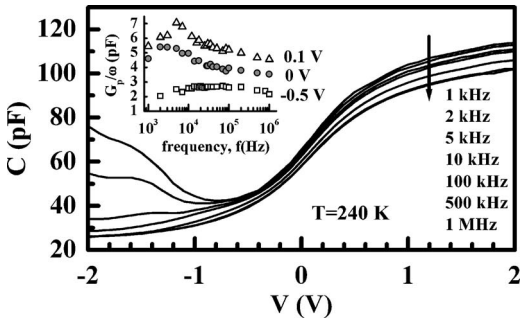

FIG. 3. Multifrequency capacitance as a function of applied gate voltage (V) measured at 240 K for a W/$LaAlO_3$/n-$In_{0.53}Ga_{0.47}As$ MOS capacitor with an area of 7.85×10^{-5} cm^2, following PDA at 500 °C in an N_2 ambient. The inset shows G_p/ω (log scale)-f for gate voltages at weak inversion (−0.5 V) and close to flatband (0,0.1 V).

in N_2 ambient. MEIS verified the absence of an IL layer.[11]

PDA at 440 °C (device I) and 500 °C (device II) for 5 min decreased t_{oxide}, indicative of dielectric film densification, and reduced frequency dispersion (<3% per decade). Figure 2 shows room temperature C-V characteristic of device II. Interestingly, the shape of the curves at frequencies <20 kHz showed a "low-frequency" (lf) behavior where the inversion layer charge starts to respond. Analogous behavior has also been reported in Ge based devices.[16,17] The minority carrier (MC) response time can plausibly be shorter in $In_{0.53}Ga_{0.47}As$ due to its smaller band gap (E_G), shorter MC lifetime (τ_L), and higher intrinsic carrier density compared to Si.[18–21] Furthermore, defects and impurities (if present) can act as sources for generation of MCs and bulk traps[18] may shorten τ_L.

Bidirectional sweep indicated hysteresis was 15–40 and 60–100 mV for devices I and II, respectively. The mechanism for the increase in hysteresis with PDA is unknown but contribution from charge centers due to outdiffusion of arsenic into the dielectric is surmised. At 1 MHz and sweep rates ranging from 3 mV/s to 10 mV/s, the hysteresis remained the same.

The upper inset of Fig. 2 compares experimental (1 MHz, device II) and the calculated ideal C-V curve.[18] Note, both the theoretical and experimental curves can have errors in the flatband to accumulation region due to the uncertainty in the measured profile near the interface and the possibility of some interface trap capacitance contribution to the measured 1 MHz curve.[18] The slope of the 1 MHz curve in depletion revealed doping of $\sim2.8\times10^{18}$ cm^{-3}. On comparison with the calculated ideal flatband voltage (V_{FB}) $\sim$0.37 V (for t_{oxide}=10.5 nm, κ_{InGaAs}=13.3, Φ_m=4.8 eV, and Φ_{InGaAs}=4.5 eV), a negative effective oxide charge of $\sim6\times10^{11}$ cm^{-2} was estimated. Due to the close agreement of the two curves, conventional Terman analysis[22] did not provide credible interface trap density (D_{it}) values. Consequently, ac-conductance method was explored.

Inset of Fig. 2 shows parallel conductance (G_p) that does not peak up in weak inversion as a function of V and shows a plateau in strong inversion. This suggests dominance of generation and recombination through bulk trap levels or through a diffusion mechanism.[18] The gate-bias independent loss also matches well with the lf behavior observed in the C-V curves. A similar characteristic has been reported in other low E_G materials.[23] However, no clear G_p peak was seen in the depletion region close to the midgap (MG).

C-V measurements on another device at 240 K exhibited C-V curves (frequency dispersion <1% per decade) with onset of lf behavior at $f<2$ kHz (Fig. 3), implying reduction of gate-bias-independent loss contribution.[16,18] The contribution of both inversion layer and interface-trap capacitances to the conductance element complicated the analysis of weak inversion G_p peak (inset, Fig. 3). Although no clear peak was seen in the depletion range near MG, D_{it} extracted for the depletion region (surface potential, $\psi_s\sim-0.1$ V) towards flatband ($\psi_{s,FB}$=0 V) is 1.5×10^{12} cm^{-2} eV^{-1}, where τ_p=0.1 ms after accounting for band bending fluctuations[18] with σ=2. Device I provided no clear G_p peak in depletion, though C-V stretch out suggested higher D_{it} than device II. Due to competing mechanisms (conductance loss in inversion and interface-state loss in depletion), still lower temperatures may be needed along with a wider frequency range to extract interface trap parameters close to MG. Furthermore, the negative charge in the surrounding dielectric can deplete the n-type surface around the periphery of the capacitor dot plausibly supplying positive carriers for inversion.[18] Device design with field isolation and different gate electrode areas[18] may be able to isolate this effect.

For a given t_{oxide} the extracted CET, without the quantum mechanical correction, remained the same for the devices with electrode areas ranging from 7.85×10^{-5} to 4.9×10^{-4} cm^2, providing a κ value of 17±1 for devices I and II [Fig. 4(a)]. The J-V characteristic revealed low gate leakage current (J_L) and scalability [Figs. 4(b) and 4(c)]. The J_L at $|V\text{-}V_{FB}|$=1 V is 4×10^{-8} A/cm^2 for 10 nm $LaAlO_3$ device I and 2×10^{-8} A/cm^2 for 10.5 nm $LaAlO_3$ device II. Both κ and J_L in our MOSCAPs are comparable to those reported for $LaAlO_3$/Si.[13]

At high applied electric field across a 10.5-nm-thick $LaAlO_3$, transport is dominated by Fowler Nordheim (FN) tunneling[24] as indicated by the linear region for both forward and reverse biases in Fig. 4(d), suggesting conduction band offset (ΔE_C) $\sim$2.2±0.2 eV between $LaAlO_3$ and InGaAs. The valence band offset (ΔE_V) $\sim$3.1±0.1 eV was extracted by the synchrotron radiation photoelectron spectroscopy.[11] Reported ΔE_V and ΔE_C for $LaAlO_3$/Si are $\sim$3.2±0.1 and 1.8±0.2 eV, respectively.[10] The oxide breakdown field is $\sim$4.3 MV/cm [Fig. 4(b)].

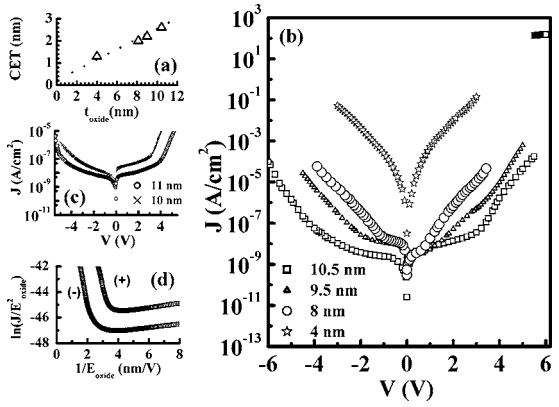

FIG. 4. (a) Capacitive equivalent thickness as a function of physical thickness (t_{oxide}) of W/$LaAlO_3$/*n*-$In_{0.53}Ga_{0.47}As$ MOSCAPs following 500 °C PDA in N_2 ambient as measured at 1 MHz. (b) Room temperature current density (J) as a function of applied gate voltage (V) and t_{oxide}. (c) J-V plot for MOSCAPs with $LaAlO_3$ annealed at 440 °C in N_2 ambient. (d) FN tunneling plot, $\ln(J/E^2_{oxide})$ vs $1/E_{oxide}$, for forward and reverse applied biases.

In summary, we observed encouraging physical and electrical characteristics such as reasonably low frequency dispersion, low leakage current density, high dielectric constant, band offsets >1 eV, and absence of an interfacial layer in amorphous $LaAlO_3/In_{0.53}Ga_{0.47}As$ MOSCAPs comparing well with $LaAlO_3$/Si devices. Additionally, gate-bias independent conductance loss was noted in inversion, implying a fast generation rate of minority carriers in *n*-$In_{0.53}Ga_{0.47}As$.

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