SmScO$_3$ thin films as an alternative gate dielectric

Citation: Applied Physics Letters 93, 052902 (2008); doi: 10.1063/1.2968660
View online: http://dx.doi.org/10.1063/1.2968660
View Table of Contents: http://scitation.aip.org/content/aip/journal/apl/93/5?ver=pdfcov
Published by the AIP Publishing

Articles you may be interested in
Amorphous lanthanum lutetium oxide thin films as an alternative high-κ gate dielectric

Gadolinium scandate thin films as an alternative gate dielectric prepared by electron beam evaporation

Structure and dielectric properties of amorphous LaAlO$_3$ and LaAlO$_x$N$_y$ films as alternative gate dielectric materials
J. Appl. Phys. 94, 1229 (2003); 10.1063/1.1586976

Epitaxial growth of yttrium-stabilized HfO$_2$ high-k gate dielectric thin films on Si

Effect of growth temperature on the properties of evaporated tantalum pentoxide thin films on silicon deposited using oxygen radicals
J. Appl. Phys. 84, 1632 (1998); 10.1063/1.368256
SmScO₃ thin films as an alternative gate dielectric

E. Durğun Özben,¹,a) J. M. J. Lopes,¹ M. Roeckerath,¹ St. Lenk,¹ B. Holländer,¹ Y. Jia,² D. G. Schlom,² J. Schubert,¹ and S. Manti¹

¹Institute for Bio- and Nanosystems (IBN-IT), Research Center Juelich, D-52425 Juelich, Germany
²Department of Materials Science and Engineering, The Pennsylvania State University, University Park, Pennsylvania 16802-5005, USA

(Received 4 June 2008; accepted 17 July 2008; published online 5 August 2008)

Samarium scandate thin films deposited on (100) Si have been investigated structurally and electrically. Rutherford backscattering spectrometry and transmission electron microscopy results show that the films are stoichiometric, amorphous, and smooth. X-ray diffraction analysis indicates that SmScO₃ starts to crystallize at 900 °C. Capacitance and leakage current measurements reveal C-V curves with negligible hysteresis, a dielectric constant around 29 for 6 nm thick films, low leakage current densities in the range of 10⁻⁷ A/cm², an effective oxide charge density of ~5 × 10¹¹ (cm⁻²), and an interface trap density of 4.5 × 10¹¹ (eV cm⁻²)⁻¹. © 2008 American Institute of Physics. [DOI: 10.1063/1.2968660]

The dielectric SiO₂ has been the key to the tremendous improvements in Si-based metal-oxide-semiconductor (MOS) device performance over the past four decades. It has, however, reached its limit in terms of scaling since it exhibits a leakage current density higher than 1 A/cm² and does not retain its intrinsic physical properties at thicknesses below 1.5 nm.¹,² In order to overcome these problems and keep Moore’s law ongoing, the use of higher dielectric constant (κ) gate oxides has been suggested. These high-κ materials must satisfy numerous requirements including high κ, large band gap and band offsets, low leakage current density, low interface trap density, high breakdown strength, acceptable reliability, and additionally thermal stability in contact with silicon. Recently, Intel reported the first 45 nm microprocessors using a hafnium-based gate oxide together with an appropriate metal gate material. The transistors in these microprocessors exhibit an order of magnitude lower gate leakage than transistors with an SiO₂ gate dielectric.³ Tomida et al. observed that Hf₁₋ₓSiₓO₂ shows different κ values depending on the crystallization phase.⁴ They observed that amorphous Hf₁₋ₓSiₓO₂ shows a κ value around 20; however, for monoclinic phase, the κ value is 15 and as they increased the temperature and changed the crystallization phase from monoclinic to tetragonal the κ value increased to 27. Moreover, Böscke et al.⁵ and Migita et al.⁶ obtained a κ of 36 and an even higher κ value for tetragonal and cubic HfO₂, respectively. However the κ of amorphous hafnium-based oxides varies between 10 and 20.⁷ In contrast, rare earth (RE) scandates (REScO₃, RE=Gd, Dy, La) show higher κ and, therefore, have attracted significant attention for high-κ applications.⁹,⁻¹³ The amorphous RE scandates have κ between 20 and 30 and the crystalline phases have κ over 30.¹² Christen et al. observed band gaps higher than 5.5 eV for these REScO₃ oxides and varying crystallization temperatures depending on the RE atomic number and the Gold-schmidt tolerance factor.¹² According to their results, the crystallization temperature of SmScO₃ (750 °C) lies intermediate between those of LaScO₃ (650 °C) and GdScO₃ (800 °C), however, among them it has the highest κ when crystallized. So far there are no experimental results about the application of amorphous SmScO₃ as a gate dielectric. The aim of this paper is therefore to establish the properties of amorphous SmScO₃ thin films concerning the above-mentioned requirements for high-κ materials.

SmScO₃ films with thicknesses ranging from 6 to 62 nm were deposited by pulsed-laser deposition (PLD) using a stoichiometric ceramic target. RCA cleaned p-type (100) Si wafers were used as substrates. Prior to film deposition the wafers were heated to 400 °C and the deposition was carried out in 2 × 10⁻³ mbar O₂ with a fluence of 2.5 J/cm² and a pulse rate of 10 Hz from a 248 nm (KrF) excimer laser. After the deposition, the structure, stoichiometry, and thermal stability of the films were investigated using Rutherford backscattering spectrometry (RBS), transmission electron microscopy (TEM), and x-ray diffraction (XRD).

For electrical characterization, MOS capacitors were fabricated. 70 nm thick Pt top contacts were deposited by electron beam evaporation through a shadow mask with areas between 2 × 10⁻⁴ and 11.5 × 10⁻⁴ cm². An Ohmic backside contact was realized by depositing 120 nm Al. Finally, the samples were annealed in forming gas (90% N₂ + 10% H₂) for 13 min at 450 °C to improve their electrical properties.

High frequency C-V measurements were carried out using an impedance analyzer (HP 4192A) at 100 kHz. The work function of the metal gate and the effective charge density in the oxide were obtained from the high frequency C-V results. The density of the interface trap states (Dₓ) was calculated using Terman’s method.¹⁴ Finally, leakage current measurements were performed using a semiconductor parameter analyzer (HP 4155B).

The stoichiometry and thickness of the films were determined by RBS. Simulation of the RBS data using the rump program¹⁵ reveals that the films have the desired stoichiometry with a ratio of Sm:Sc:O = 1:1:3.

A cross-sectional TEM image of a 49 nm thick SmScO₃ film on Si (100) (Fig. 1) shows an amorphous and smooth film on Si. The figure also indicates the existence of an interfacial layer between the silicon and the high-κ dielectric

---

³Electronic mail: eylemdurgun@gmail.com.
with a thickness of 2.5 nm. The growth of the interfacial layer is probably related to the oxidation of the silicon surface during PLD growth.

In order to study the thermal stability of the SmScO₃ grown at 400 °C, rapid thermal annealing in ultrapure N₂ was performed at atmospheric pressure and different temperatures ranging from 700 to 1100 °C for 10 s. Figure 2 shows the XRD patterns of a 22 nm thick SmScO₃ film for different annealing temperatures. It is apparent that the as-deposited film is amorphous, in agreement with the TEM results. The film remains amorphous up to 800 °C and the crystallization of the orthorhombic SmScO₃ phase starts at 900 °C, as indicated by the arrows identifying SmScO₃ reflections. The value for the onset of crystallization is higher than that for HfO₂ (Ref. 16) and comparable to Hf silicates.17

It is, however, lower than for DyScO₃ and GdScO₃.10

Figure 3 shows the capacitance normalized to the gate area versus gate voltage for SmScO₃ films with different thicknesses. The C-V curves are smooth and free of humps. Double sweep measurements from inversion to accumulation and back were carried out at a frequency of 100 kHz with a 3 s hold time for each measuring point. Negligible counter clockwise hysteresis indicates that these samples contain a low density of positive trap charges, \( Q_{\text{ox}} \), in the range of \( \sim 10^{10} \) cm\(^{-2} \), as estimated from the simple formula, \( Q_{\text{ox}} = (C_{\text{ox}}/q)\Delta V_{\text{FB}} \), where \( C_{\text{ox}} \) is the accumulation capacitance normalized to the gate area, \( q \) is the electron charge, and \( \Delta V_{\text{FB}} \) is the voltage shift from the reverse bias measurement to the forward one.

Using the curves shown in Fig. 3, the capacitance equivalent thickness (CET) was extracted from the capacitance in the accumulation region \( C_{\text{acc}} \) as CET = \( A\varepsilon_0\kappa_{\text{SiO}_2}/C_{\text{acc}} \), where \( A \) is the gate area, \( \varepsilon_0 \) is the permittivity of vacuum and \( \kappa_{\text{SiO}_2} \) dielectric constant of SiO₂. Figure 4 shows a plot of the CET versus oxide thickness \( t_{\text{ox}} \). From the slope of the linear fit, it is possible to extract the dielectric constant of the films disregarding the contribution of the interfacial layer. The \( \kappa \) thus obtained for amorphous SmScO₃ is \( \sim 29 \). The intercept of the line with the CET axis represents the electrical thickness of the lower-\( \kappa \) interfacial layer, which is found to be 2.5 nm. This value is in agreement with the physical interfacial layer thickness observed by TEM indicating that this layer has a \( \kappa \) comparable to SiO₂ and thus likely is SiO₂.

The flatband voltage (\( V_{\text{FB}} \)) of the samples has been extracted from the comparison between the ideal C-V curves and experimental ones obtained from the capacitors exposed to forming gas annealing at 450 °C. The sample with a 6 nm thick SmScO₃ oxide layer has a \( \sim 0.1 \) V flatband shift and as the thickness of the oxide layer increases the flatband voltage shifts to more negative voltages. In order to evaluate the effective oxide charge density (\( N_{\text{eff}} \)) and the effective work function of the Pt metal gate (\( \Phi_{\text{m,eff}} \)), \( V_{\text{FB}}+\Phi_{\text{y}} \) versus CET was plotted in Fig. 5, where \( \Phi_{\text{y}} \) is the work function of the silicon. \( V_{\text{FB}} \) can be expressed as19

\[
V_{\text{FB}} = \Phi_{\text{m,eff}} - \Phi_{\text{y}} - qN_{\text{eff}}(\text{CET}/\varepsilon_0\kappa_{\text{SiO}_2}),
\]

where \( N_{\text{eff}} \) does not change with the oxide layer thickness.
were calculated using Terman’s method. The values are to be 4.84 eV. This value satisfies the work function requirement of the high in the oxide layer.

5 start to crystallize at 900 °C. The results indicate low oxide C smooth and a

with a 6 nm thick SmScO₃ it is in the range of 10⁻⁷ A/cm² and, for thicker films, it is even below the detection limit of the measurement system for the contact size used.

We have investigated the thermal stability and electrical properties of SmScO₃ thin films and their interface to Si (100). The films remain amorphous on Si up to 800 °C and start to crystallize at 900 °C. The results indicate low oxide charge and interface trap charge densities in the range of 5 x 10¹¹ cm⁻² and 4.5 x 10¹¹ (eV cm⁻²)⁻¹, respectively. Very smooth C-V curves with negligible hysteresis were recorded and a κ value of ~29 was extracted from the electrical measurements. The films reveal low leakage current densities in the range of 10⁻⁷ A/cm² for 6 nm thick film. It can be concluded that amorphous SmScO₃ shows promising properties as an alternative high-κ gate dielectric, which might allow it to be used in future integrated circuits.

![Graph showing V_Fb + Φ_s vs CET.](image)

**FIG. 5.** V_Fb + Φ_s vs CET. The intercept of the best-fit line on the V_Fb + Φ_s axis gives φ_{m,eff} and the slope N_{eff}.

From the intercept of the V_Fb + Φ_s axis, φ_{m,eff} was found to be 4.84 eV. This value satisfies the work function requirement for a p-type MOS field-effect transistor. From the slope of the curve N_{eff} was evaluated to be 5 x 10¹¹ cm⁻². Such a low charge density indicates a low concentration of defects in the oxide layer.

Another important issue for MOS capacitors is the quality of the high κ/Si interface. To evaluate the quality of the Si/SmScO₃ interface after forming gas annealing, D_it levels were calculated using Terman’s method. The values are ~4.5 x 10¹¹ (eV cm²)⁻¹ and do not show a clear dependence on the oxide thickness, as expected. Finally, the leakage current density of the samples was measured. For the sample with a 6 nm thick SmScO₃ it is in the range of 10⁻⁷ A/cm² and, for thicker films, it is even below the detection limit of the measurement system for the contact size used.

We have investigated the thermal stability and electrical properties of SmScO₃ thin films and their interface to Si (100). The films remain amorphous on Si up to 800 °C and start to crystallize at 900 °C. The results indicate low oxide charge and interface trap charge densities in the range of 5 x 10¹¹ cm⁻² and 4.5 x 10¹¹ (eV cm⁻²)⁻¹, respectively. Very smooth C-V curves with negligible hysteresis were recorded and a κ value of ~29 was extracted from the electrical measurements. The films reveal low leakage current densities in the range of 10⁻⁷ A/cm² for 6 nm thick film. It can be concluded that amorphous SmScO₃ shows promising properties as an alternative high-κ gate dielectric, which might allow it to be used in future integrated circuits.